FABRICATION AND ANALYSIS OF LATERAL SCHOTTKY BARRIER SOLAR CELL

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By
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CERTIFICATE

This is to certify that the thesis entitled, 'Fabrication and Analysis of Lateral Schottky Barrier Solar Cell' by Rajeeva Lahri is a record of work carried out under my supervision and has not been submitted elsewhere for a degree.

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Rajeeva Lahri

CONTENTS

LIST OF SYMBOLS

I_{sc}	Photo current due to radiation or short circuit current (same as I_s or I_L)
I_o	Reverse saturation current
A^*	Richardson's constant
V_{oc}	Open circuit voltage
V_{mp}, I_{mp}	Voltage and current corresponding to maximum powe
n	Ideality factor
q	Electronic charge
k	Boltzmann's constant
R_s	Series resistance
L	Grid spacing
B	Grid width
N	Number of incident photons per unit area per unit time
α	Absorption coefficient

SYNOPSIS

In the present work, a new grid structure for Schottky Barrier Solar Cells (SBSCs) has been fabricated and analysed. The motivation for this work was to eliminate the use of thin metal-films in SBSCs. These thin films affect the reliability and reproducibility of the device. Moreover, a deterioration in the quality of such films, with time, is expected because of the thermal cycling that these films would undergo during the operation of the cell.

The feasibility of the structure is experimentally established. The present low efficiency of the cell is attributed to the non-optimised grid structure and the absence of anti-reflection coating.

Furthermore, a theoretical analysis of the above structure is carried out to optimise the grid structure and study the effect of certain parameters like surface recombination and series resistance on the performance of the cell. The ratio (L/B) of the grid spacing (L) to grid width (B) is found to be a very useful parameter in characterising the structure. Calculations are done to study the variation of cell efficiency with the parameter L/B. The efficiencies

are found to be lower than the corresponding values reported in the literature. This is due to thefact that, in the present calculations, a first order account of the recombination of minority carriers in the bulk semiconductor has been taken.

Calculations are also done to find the optimum thickness of antireflection coating for the cell.

CHAPTER I

INTRODUCTION

1.1 SOLAR ENERGY AND ITS PROSPECTS

There are certain trends which combine to cause concern over the future availability of energy. These contributing factors include the forecast of exponential growth in energy consumption, especially in the portion of energy used as electricity; the depletion of oil and gas reserves and the concern for environmental protection.

Fusion, geothermal, solar and organic wastes seem to be the only alternatives for future energy sources. However, each of them has, at present, certain limiting aspects regarding its technical feasibility and engineering realizability. These problems have to be solved before we can look forward for their utilization in large scale power generation.

Out of these, solar energy is the most promising, as it is available in abundance. For example, in India, the net solar radiation is around 400 Watt/meter^2[1]. Besides this, its utilization leaves no waste products, thereby avoiding pollution problems. Possible ways to use

solar energy are through photovoltaic semiconductor devices for direct conversion of solar energy to electricity high temperature solar heat concentrators for power generation, low temperature heat generation by flat plate collecto. for space heating and production of chemical fuels by photo synthesis. In order to utilise solar energy during night and long overcast periods, one has to employ storage devices. Heat storage in water, rocks and phase-change materials has been demonstrated. Similarly, batteries for storing electrical power have also been tried.

Power generation from sun for space applications requires high efficiency of the system irrespective of its cost. However, for terrestrial applications, cost becomes a major consideration even at the expense of efficiency. The use of solar energy in the generation of electrical power is limited by two factors: low intensity of solar radiation and its intermittancy. Thus, along with the cell, the cost for concentrators, storage and supporting structures has also to be considered. The cost of power generation through photovoltaic cells is around $ 30,000/KW [2]. This when compared with the cost of fossil fuels ($ 1000-3000/KW)sh that the cost of photovoltaic cells should be reduced, atleast, by a factor of ten in order to make them competitive with conventional fuels. A significant cost-reduction may be

achieved if purified, 'polycrystalline' silicon ($14.80/m^2), instead of silicon single crystals ($43/m^2), is used [3]. The feasibility of the use of 'polycrystalline silicon on a cheap substrate' has been demonstrated by Chu etal.[4]. The efficiency of the cell was .05 %. An improvement in the efficiency, to 6.2 %, was observed by using silicon ribbons [5

Only recently, Solarex Corporation of Rockville, Md., has reported that 'terrestrial conversion efficiencies of 10 % have been obtained with solar cells developed from impure, potentially inexpensive semicrystalline silicon'.[6] This development is highly significant, because the high price of single-crystal silicon is a major deterrent in the manufacture of inexpensive solar cells and a cheaper cell, with a reasonably high efficiency of 10 %, can have a tremendous impact on the use of solar cells as a primary source of electrical power.

1.2 SOLAR CELLS:

A solar cell works on the principle of photovoltaic effect, which is the conversion of electromagnetic radiation to electrical energy through optical excitations in semiconductors. When a photon of sufficient energy is incident on a semiconductor, electron-hole pairs (e-h pairs) are generated. These pairs, if separated and made to flow through an external circuit, give rise to electric current. The

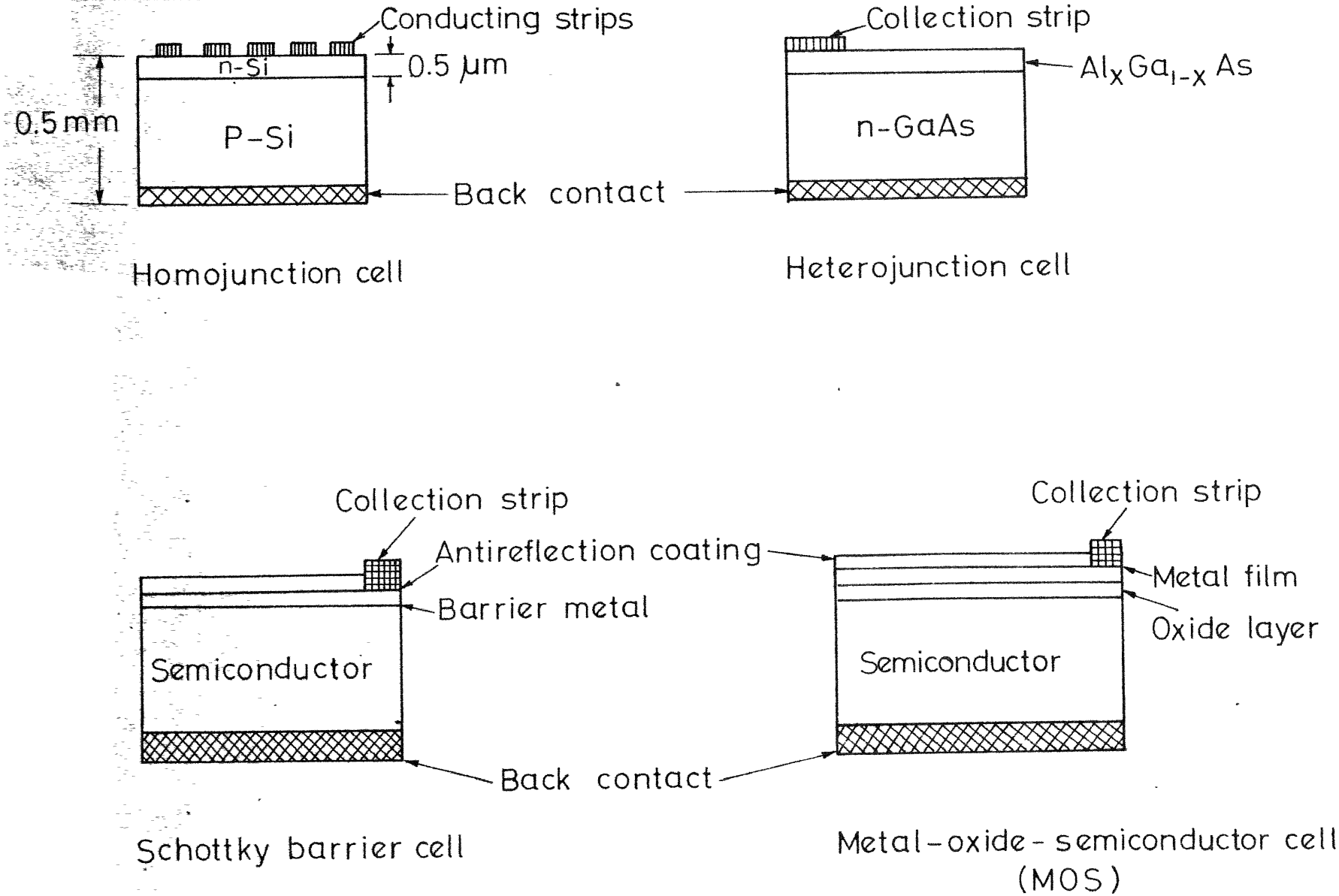


FIG. 1.1 TYPICAL STRUCTURES OF SOLAR CELLS

current through an external resistor means electrical power output as a result of the incident radiation input. In solar cells, the pair separation is done by the built-in electric field in the device. These built-in electric fields are present at the junction of either two different resistivity regions of the same semiconductor (high-low junctions), or two different conductivity types of the same semiconductors (homojunction), or two different semiconductors (heterojunction) or a metal and a semiconductor (Schottky Barrier). Depending on the type of junctions, solar cells can be classified accordingly. However, there are following four categories which have been studied extensively: Homojunction, Heterojunction, Schottky Barrier and Metal-Oxide-Semiconductors (MOS) solar cell. Typical structures of each type is shown in Fig. 1.1.

(a) Homojunction Solar Cells:

These cells are large area p-n junctions made from the same material. The first homojunction solar cell was developed by Chapin, Pearson and Fuller in 1954 [7]. Though, GaAs, InP etc. have also been tried, silicon is the most used material in the fabrication of solar cells and has given the best overall efficiency of 14% [8]. p-n junction solar cells are commercially available and have efficiency around 10%.

(b) Heterojunction Solar Cells:

These cells are fabricated by using two semiconductors of different band gaps, to facilitate more effective utilization of solar radiation. However, the disadvantage of this system is that the maximum open circuit voltage is less than the smaller of the two band gaps. Also, the mismatch in lattice parameters of the two materials gives rise to interface states within the energy gap, thereby enhancing the recombination of charge carriers. This reduces the conversion efficiency.

An efficiency of 17.5 %, with concentrators (effective concentration 312 suns), in Al_x Ga_{1-x} As/GaAs system has been reported [9]. In literature, a large number of other heterojunction cells are reported. A few examples are: Cu_2S-Cds [10-1 Se-Cds [12] and InP-Cds [13]. Only recently, the fabrication of a polycrystalline thin film InP-Cds solar cell of area .52 mm^2 having a power conversion efficiency of 2.8 % under AMI conditions (93 mW/cm^2) have been reported [14].

(c) Schottky Barrier Solar Cells:

Schottky Barrier Solar Cells (SBSCs) are, essentially, metal semiconductor junction cells where a thin film of metal is deposited on a semiconductor and, then, the back ohmic contacts are made. The cells seem to be very promising due to their inherent advantages over conventional, commercially

available p-n junction solar cells. These advantages are discussed in the next section.

In 1974, Anderson etal.[15] reported 8.1 %efficient SBSC, and, in 1975, Anderson and Milano [16] reported 9.5 % efficient SBSC.

(d) MOS Solar Cells:

A considerable activity has started in this field as a result of the studies on the role of interfacial layers in SBSC. These interfacial layers (usually oxides) tend to increase the open circuit voltage, and, hence, the efficiency of the system. In MOS, a thin oxide layer ($\sim$23 Å) is grown on a single-crystal semiconductor and, then a metal film is deposited. Strin and Yeh [17] have reported 15% efficient antireflection coated GaAs MOS Solar Cells. Similarly, Charlson and Lein [18] have reported 8% efficient Aluminium-p-type silicon MOS Solar Cells.

1.3 COMPARISON OF SBSCs AND HOMOJUNCTION SOLAR CELLS:

The greater simplicity of fabrication and lower cost as compared to homojunction solar cells makes SBSC an attractive proposition for both space and terrestrial applications. Also, the maximum theoretical efficiency of a silicon SBSC (24.4%) is slightly higher than that of a silicon homojunction cell (22%)[19].

Only those e-h pairs, which are generated within a diffusion length of minority carriers from the depletion region, reach the junction and get separated there. Obviously then, for better collection efficiency most of the pair generation should take place near the depletion region. In homojunction cells, the depletion region lies at the junction. Therefore, it should be as shallow as possible. Fabrication of shallow junctions poses technical difficulties, which are obviated in SBSCs since, in this case, the depletion region lies at the metal semiconductor interface; this also leads to a better shortwave response in the case of SBSC's as compared to homojunction cells.

The high temperature diffusion process, involved in the fabrication of a homojunction cell, degrades the quality of the semiconductor, thereby reducing the minority carrier life time. This degradation does not occur in SBSCs as these are fabricated by a low temperature process.

Moreover, SBSC structures, contrary to homojunction cell structure, can be made use of in polycrystalline semiconductors. This, as has been discussed in sec. 1.1 may significantly reduce the cost of power generation.

1.4 EQUIVALENT CIRCUIT FOR SCHOTTKY BARRIER SOLAR CELLS:

The photovoltaic conversion, in the case of SBSC, may be represented by a Schottky diode with a constant current source in parallel with it. The latter results from the excitation of an excess of carriers, over their thermal equilibrium concentration, and their diffusion and drift across the barrier. The equivalent model is shown in Fig. 1.2

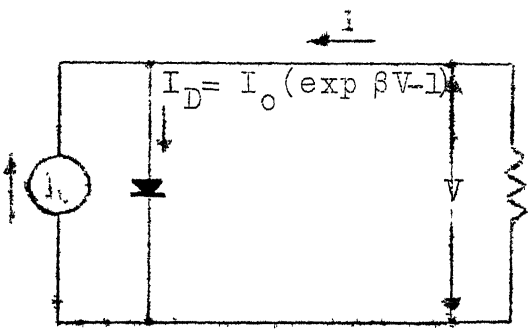


Fig.1.2: Equivalent Model for an ideal SBSC

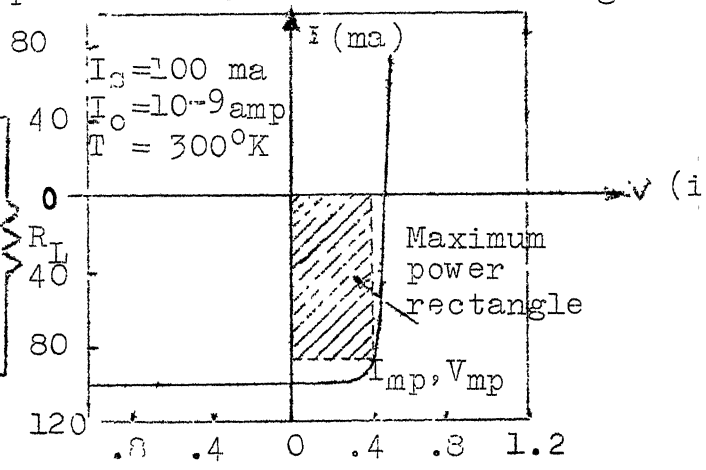


Fig.1.3: I-V Characteristics of an ideal SBSC

The I-V characteristics of such a device are given by,

$$I = I_o(e^{\beta V} - 1) - I_s \qquad (1.1)$$

$$I_o = aA^* T^2 \exp(-q\varphi_B/kT) \qquad (1.2)$$

where, $\beta \equiv q/nkT$

A^* = Richardson's constant

I_o is the saturation current, I_s is the photogenerated current, V is the diode voltage, a is the diode area, φ_B is the metal-semiconductor barrier height, and q, k and T have their usual meanings.

A plot of equation (1.1) is given in Fig. 1.3. Since the curve posses through the fourth quadrant, power can be extracted from the device. The area under the curve in fourth quadrant gives the total amount of extractable power. However, the power transferred to the external resistor depends upon the operating point (i.e. the value of the load resistance). By properly choosing a load, for maximum power transfer (characterised by the operating point (I_{mp}, V_{mp})), it is possible to extract close to 80% of the product I_{sc} x V_{oc}, where I_{sc} is the short circuit current and V_{oc} is the open circuit voltage of the cell. It is indicated by the maximum power rectangle in Fig. 1.3. The ratio of maximum power transferable to the total extractable power from a solar cell is termed as 'curve factor' or 'fill factor'.

From eqn. (1.1) we get the open circuit voltage,

$$V_{oc} \equiv V_{max.} = \frac{1}{\beta} \ln \left(\frac{I_s}{I_o} + 1\right) \qquad (1.3)$$

The output power is given by,

$$P = IV = I_o V(e^{\beta V} - 1) - I_s V \qquad (1.4)$$

The condition for maximum power can be obtained when $\frac{\partial P}{\partial V} = 0$, or

$$(1+\beta)\exp(\beta V_{mp}) = \left(1 + \frac{I_s}{I_o}\right) \tag{1.5}$$

and,

$$I_{mp} = I_o (e^{\beta V_{mp}} - 1) - I_s = I_o \beta V_{mp} e^{\beta V_{mp}} \tag{1.6}$$

The conversion efficiency (η) is given by,

$$\eta = \frac{\text{max. power output}}{\text{power input}} = \frac{I_{mp} \times V_{mp} \text{ (per cm}^2\text{)}}{P_{in} \text{ (per cm}^2\text{)}} \tag{1.7}$$

$$= \frac{I_s \beta V_{mp}^2}{(1 + \beta V_{mp})A} \left(1 + \frac{I_s}{I_o}\right) \frac{1}{P_{in} \text{ (per cm}^2\text{)}} \tag{1.8}$$

where, A is the exposed area of the SBSC and P_{in} is the solar power density. P_{in} is around 1 KW/m^2 at sea level.

However, in practice, the cell may have a resistance (R_{sh}) due to surface leakage, shunting the Schottky diode and a resistance (R_s), due to bulk resistance of the semiconductor, sheet resistance of the thin metal film, contact resistance etc., in series with the above combination. Therefore, the equivalent circuit of an actual SBSC can be represented as shown in Fig. 1.4.

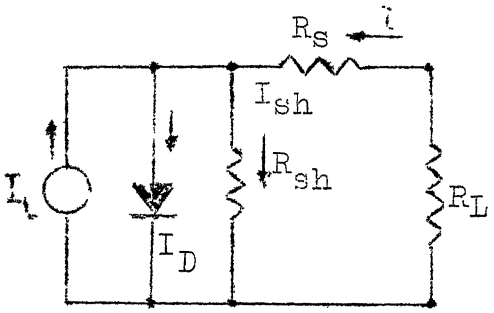


Fig.1.4: Equivalent Model for an actual SBSC.

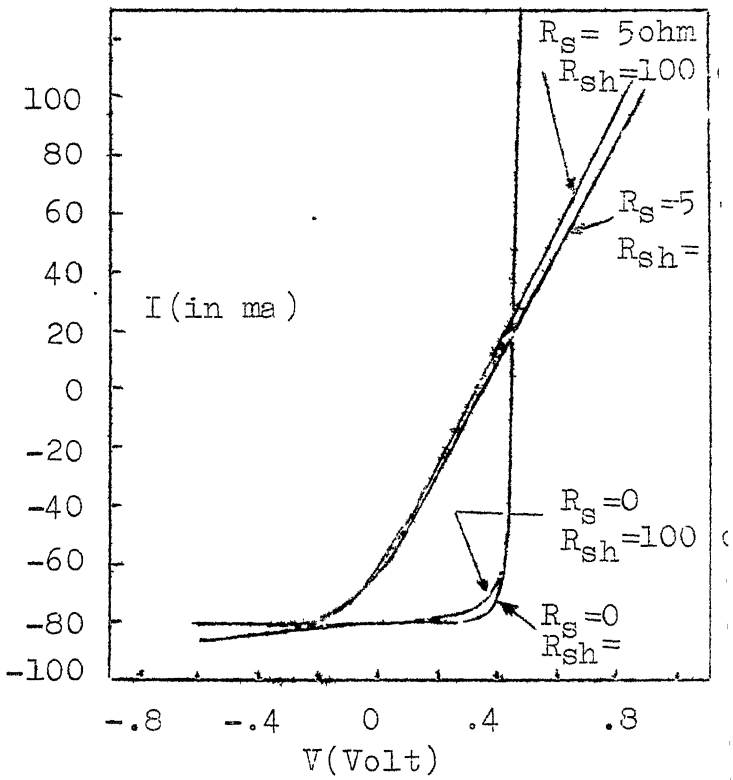


Fig.1.5: I-V characteristics of a SBSC with R_s and as parameters.

The I-V characteristics of the above model are given by,

$$\ln\left[\frac{I + I_s}{I_o} - \frac{V - IR_s}{I_o R_{sh}} + 1\right] = \beta (V - IR_s) \qquad (1.9)$$

Plots of eqn. (1.9) with various combinations of R_s and R_{sh} are given in Fig. 1.5.

As is evident from Fig. 1.5, a shunt resistance as low as 100 ohms does not appreciably alter the power output, whereas a series resistance of only 5 ohms reduces the power available to less than 30% of the maximum power with $R_s = 0$. Since R_{sh} does not significantly affects results, it may be neglected. Thus equation (1.9) can be rewritten as,

$$\ln \left[\frac{I + I_s}{I_o} + 1 \right] = \beta (V - IR_s) \qquad (1.10)$$

The output power would be,

$$P = IV = I \left[\beta \ln \left(\frac{I + I_s}{I_o} + 1 \right) + IR_s \right] \qquad (1.11)$$

The relative maximum power is 1, .77, .57, .14, .07 for series resistances of 0, 1, 2, 5, 10, 20 ohms respectively [20].

1.5 DISCUSSION ON THE SERIES RESISTANCE:

The drastic deterioration in the performance of a solar cell with the increase of its series resistance has already been emphasised in sec. 1.4. Minimisation of this resistance is, at present, a major technological problem. This effect becomes more acute when higher illumination intensities are used, with the help of a concentrator system.

In SBSC, the carriers generated, due to the incident radiation, in the bulk-semiconductor diffuse to the metal-semiconductor junction and get separated by the electric field of the space-charge region. If the semiconductor is p-type, the separated minority carriers (electrons) would enter the thin metal film. However, if it is on n-type semiconductor, the minority carriers (holes) at the junction would recombine with the electrons flowing from the

metal film. The driving force for these minority carriers arises from the differences in the quasi-fermi level of the minority carriers and the fermi level of the semiconductor. Therefore, the carriers move towards or away from the collecting strip, depending on the type of minority carriers (as explained earlier) and contribute to the current through the external circuit (cf. Fig. 1.1). The resistance faced by these carriers is dependent on the location where they enter the thin metal-film. Therefore, the resistance is determined by a non-uniform current distribution and may be termed as a 'distributed resistance'. Other resistances can belumped together as they are uniformly traversed by the current flowing through the cell. These comprise of the resistances of the contact strip, bulk-semiconductor, bottom electrode and the contact resistance of the bulk semiconductor to the bottom electrode.

Contribution to series resistance due to the above distributed resistance would be greatly minimised if the average path length of the injected carriers is reduced by putting more strips for collection. This principle is made use of in grid structures. A typical grid structure is shown in Fig. 1.6.

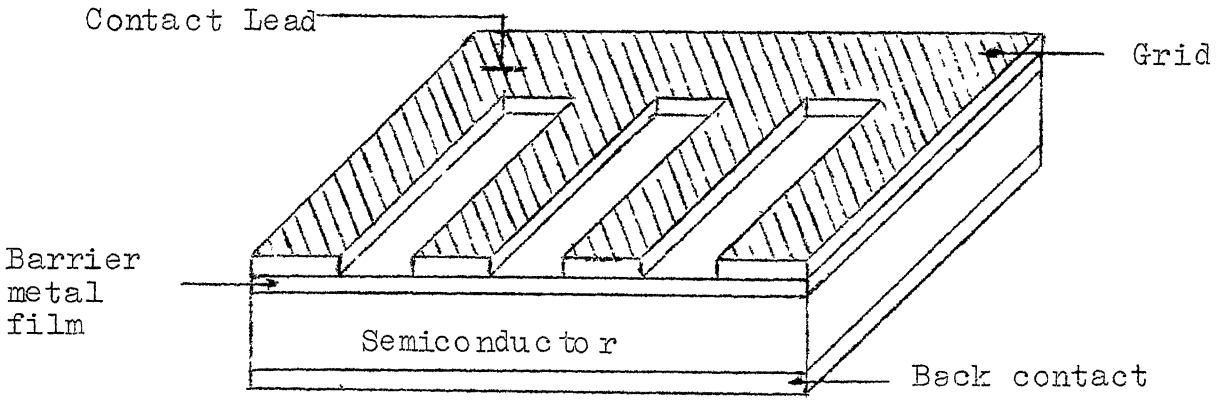


Fig. 1.6: A typical grid structure for SBSC.

For the current flow in the external circuit, the carriers collected by the grid strips have to travel all the way to the contact lead. Therefore, the sheet resistance of the grid strips should be very small. This requires thick and wide grid strips. But, the area under the thick grid strip would not contribute anything to current generation, as all the incident radiation, in that area, would be absorbed by the metallic grid itself. Therefore, the active area of the cell would be reduced. This puts an upper limit to the number and size of the grids for optimum cell performance. Such calculations have been performed by Handy [22], Jain and Stuber [23] and Lamorte [24].

The back contact resistance to bulk semiconductor can be eliminated altogether by using special alloys meant for ohmic contacts. For example, for n-type silicon, Au-Sb alloy can be used. The contacts can also be made ohmic if they are made on a rough surface so that the injected minority carriers

recombine in the traps themselves. The resistance of the bulk semiconductor can be minimised by using epitaxial wafers. This allows to have two layers of different resistivity on the same wafer ($n-n^+$ or $p-p^+$). The top layer is less doped, commensurate with low reverse saturation current and the bottom layer is highly doped to give low resistivity.

The gridded structures are being regularly employed in p-n junction and Schottky Barrier Solar Cells.

1.6 LATERAL SCHOTTKY BARRIER SOLAR CELL:

As mentioned in sec. 1.4, the use of thin barrier metal films may lead to deterioration, with time, in the performance of SBSCs due to thermal cycling that the cell undergoes during its operation. Also, the evaporation of thin metal films puts certain rigid constraints on the fabrication process. These two factor affect the reliability and reproducibility of the device respectively.

The motivation for the structure, to be described here, is the need to obviate the use of thin metal films in SBSCs. The structure was first suggested by Green [25] in Sept. 1975. In this structure, the radiation is incident directly on the semiconductor. The generated carriers are collected by conducting metallic strips which provide the Schottky Barrier for pair separation. A schematic diagram

of the structure is shown in Fig. 1.7.

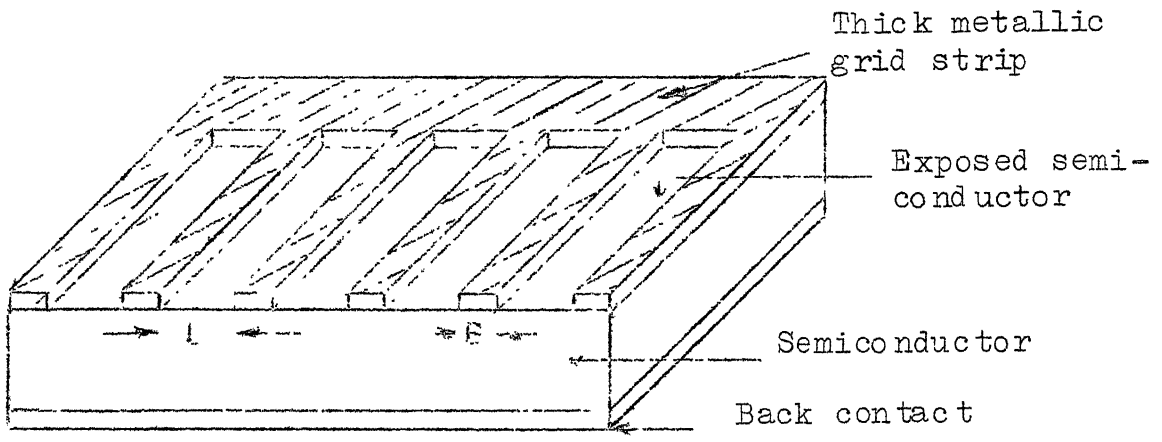


Fig.1.7: Schematic diagram of lateral SBSC.

Here, it must be emphasised that the structure in Fig. 1.7 is entirely different from the one in Fig. 1.6. In the structure shown in Fig. 1.6, the barrier metal film covers whole of the semiconductor surface and the pair separation takes place at the metal-semiconductor junction. The grid strips merely act as collecting strips; whereas, in the structure shown in Fig. 1.7, the grid strips serve the purpose of metal-semiconductor contact and also act as collecting strips. The advantages and disadvantages of this structure are discussed later in this section.

Since, the carriers in this case diffuse laterally to the grid strips for collection, the structure may be termed as LATERAL SCHOTTKY BARRIER SOLAR CELL (Lateral SBSC).

In conventional SBSC, (cf. Fig. 1.1), the incident radiation passes, through the metal film, to the semiconductor

and the minority carriers, subsequently generated, are collected by the contact strip. Therefore, the active collecting area (Aa), the area of contact (Ac) and the geometrical area (Ag) are all equal in this case. In lateral SBSC, if the grids cover only a small fraction of the surface, Aa would be slightly smaller than Ag while Ac would be much smaller than Ag. Therefore, the light generated current (I_s) would go down slightly but I_o would be decreased substantially.

Green has shown that the open circuit voltage, due to anxincrease in I_o (cf. eqn. 1.3) would more than compensate any decrease in I_s due to the decreased surface area. The sheet resistance of the grid strips is not likely to pose any problem as the strips can be made sufficiently thick. Therefore, an increase in the cell-efficiency is to be expected. Fig. 1.8 shows a comparison of the conversion efficiency of conventional and lateral SBSC. Here, the factor L/B is chosen in such a way that L is always less than twice the minority carrier diffusion length.

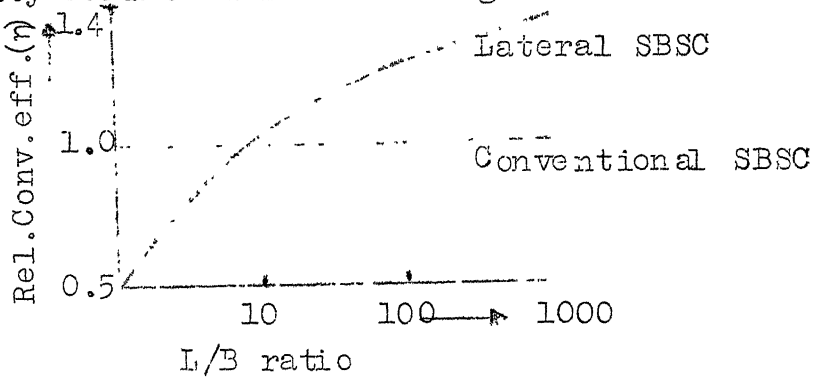


Fig. 1.8: Variation of η with L/B ratio.

The major practical limitation of the new geometry arises from the necessity of having very narrowly spaced grid strips. For effective collection of carriers, the spacing (L) should be less than twice the minority carrier diffusion length. The value of L is normally around 100 μm for p-type silicon. From Fig. 1.8 we see that for better relative conversion efficiency of lateral SBSC over conventional SBSC, L/B should be greater than 8. This calls for extremely small values of B. Standard photolithography techniques, described in the next chapter can produce values of B only upto 2μm. It should be noted, however, that there are sophisticated photolithography techniques available to provide resolution upto .01 μm. However, the added process of photolithography adds to the cost of these type of cells. The evaporation of thick metal films put less rigid constraints on the reproducibility and reliability of the device. Also, the use of thick metal films provides some other advantages like proper heat treatment for silicide formation etc. These are discussed, in detail, later.

CHAPTER II

DEVICE FABRICATION

2.1 THE FABRICATED SYSTEM:

In the present work, the main concern has been to test the feasibility of the gridded structure described in sec. 1.7. So far, no attempt has been made to optimise the parameters involved to increase the efficiency. These parameters have been chosen arbitrarily, in accordance with the existing facilities in the laboratory. The gridded structure is made by cutting windows in an aluminised silicon wafer. The windows are cut, in the thick Al-film, using standard photolithographic techniques. The process is described in the next section. The grid width and grid spacing are 75 μm and 375 μm respectively. The back contact is made by evaporating thick aluminium on the unpolished back surface. Copper leads are taken out, by using silver paint, from both the front and the back surfaces.

2.2 STEPS IN THE FABRICATION:

Following are the steps, in sequence, followed in the fabrication of the device:

(a) Wafer Preparation:

The silicon slices, used in the fabrication of the device, are n-type with nominal resistivity of 1 ohm.cm. They are polished on the front surface and lapped on the back surface. The first step isto cut the wafer into 1 x 1 cm pieces. This is done by scribing lines, one cm. in spacing, on on the whole slice, with a diamond scriber, along and perpendicular to <111> direction. Then, the scribed wafer is put in a dust-free polythene bag and slightly pressed. The wafer breaks along the scribed lines, as <111> is the easy axis in silicon single crystals. After this, the pieces are thoroughly rinsed with deionised (DI) water to remove any dust that might have generated during scribing.

(b) Wafer Cleaning:

The cut wafers are cleaned by first degreasing them with Trichloroethylene (TCE), Acetone and Methanol respectively. Then they are oxidised in conc. Nitric acid. The oxide layer is etched away using Hydrofluoric acid. A flow chart of the process is given in Fig. 2.1. Then, the wafer is transferred to the vacuum chamber in a ground glass-sealed container.

(c) Metal Cleaning:

The metal used for evaporation is aluminium. It is first degreased with TCE, Acetone and Methanol respectively.

Then it is etched for about 5 seconds in dilute orthophosphoric acid.

(d) Aluminization:

Once completely cleaned, the whole surface of the wafer is covered with about 5000 Å of aluminium by the standard vacuum deposition technique. The silicon wafers are held polished side down in a holder. Beneath this, in a heater filament (tungsten), several small pieces of cleaned aluminium strips are hung. When the bell jar is pumped down to 5×10^{-5} Torr, the filament current is turned on sufficiently to melt the aluminium. When the aluminium has melted, the silicon wafer is exposed to the flux of aluminium atoms by opening the shutter between the wafer and the filament. Then the current is increased further to some predetermined value until all the aluminium has evaporated. The chamber pressure was not allowed to go above 10^{-4} Torr during this period. After the system cools down for a few minutes, it is opened to atmospheric pressure and the aluminized water removed. Since, in this process, the thickness is not crucial, it can simply be controlled by the amount of aluminium wire hung on the filament.

(e) Heat Treatment:

The aluminized silicon wafer is kept at $525^{\circ}C$ for 15 minutes in a quartz tube and then cooled down slowly, at

a rate of 3-4°C/min. During the whole process, ultrapure argon is passed so that the sample may not get oxidised.

(f) Photolithography:

Aluminium photolithography is a standard technique used widely in I.C. industries. The mask needed for photolithography was made on a glass slide. The process of mask preparation is described later in this section. A detailed flow-chart of the photolithography is given in Fig. 2.2.

In photolithography, the freshly prepared aluminiumized silicon surface is covered with KMER photoresist. The mask is super imposed on the aluminized surface and exposed to ultraviolet radiation. During exposure, the exposed part is polymerised while the unexposed portion remains unaffected. Later, after developing the image, the unaffected photoresist is removed by a mixture of Isopropyl alcohol and KMER Thinner (1:8). Therefore, the final pattern consists of polymerised photoresist strips with bare aluminium in between.

(g) Aluminium Etching:

The bare aluminium is etched away using aluminium photoresist (See Fig. 2.3). This process is very critical as 'under-cutting' of the photoresist strips may occur. The procedure to avoid undercutting is discussed in sec. 2.3.

(h) Photoresist Removal:

Polymerised photoresist is removed by swiping it with warm Baker's photo-stripper. Utmost care has to be taken during this step, otherwise aluminium may peel-off during swiping.

(i) Back Contact Evaporation:

The back surface is first swiped with TCE, Acetone and Methanol respectively. This is to remove any greasy substance sticking on the surface. After this, the oxide, if any, is etched away by swiping the surface with hydrofluoric acid. Care has to be taken during this process to avoid spilling of HF onto the front surface. After this, aluminium is evaporated by the usual vacuum evaporation technique described earlier.

(j) Lead Attachment:

Copper leads are attached to the front and back surface with the help of silver paint To make the contact more rigid, a drop of areldite is put to cover the silver paint.

A flow diagram of the device fabrication is shown in Fig. 2.3.

Mask Preparation:

The mask needed for photolithography should be prepared by first drawing the original geometries on a mylar sheet and,

then, reducing them photographically to the desired dimensions. However, due to the lack of these facilities, the mask was fabricated as follows:

Firstly a 2 in. x 2 in. glass slide is cleaned thoroughly with soap solution and chromic acid and then a thick layer (10,000 Å) of aluminium is deposited, in vacuum, using the standard vacuum deposition technique. After this, with a diamond scriber, parallel lines are scribed on the aluminized glass surface. This removes the aluminium from the scribed portions. Therefore the ultimate pattern consists of transparent lines with opaque aluminium strips in between. At the top of the pattern, whole of the aluminium is removed by swiping with acetone. This corresponds to the contact strips in the lateral SBSC. The transparent lines correspond to thegrids and their width gives the value of B. Similarly the opaque region is the exposed silicon surface with width L (cf. Fig. 1.7). In the actual fabrication, L and B were 375 μm and 75 μm respectively.

2.3 DISCUSSION ON THE FABRICATION PROCESS:

The above process of device fabrication was repeated several times to standardise the timings and other parameters involved in various steps. Moreover, the affect of alteration in certain parameters on the ultimate device was also observed.

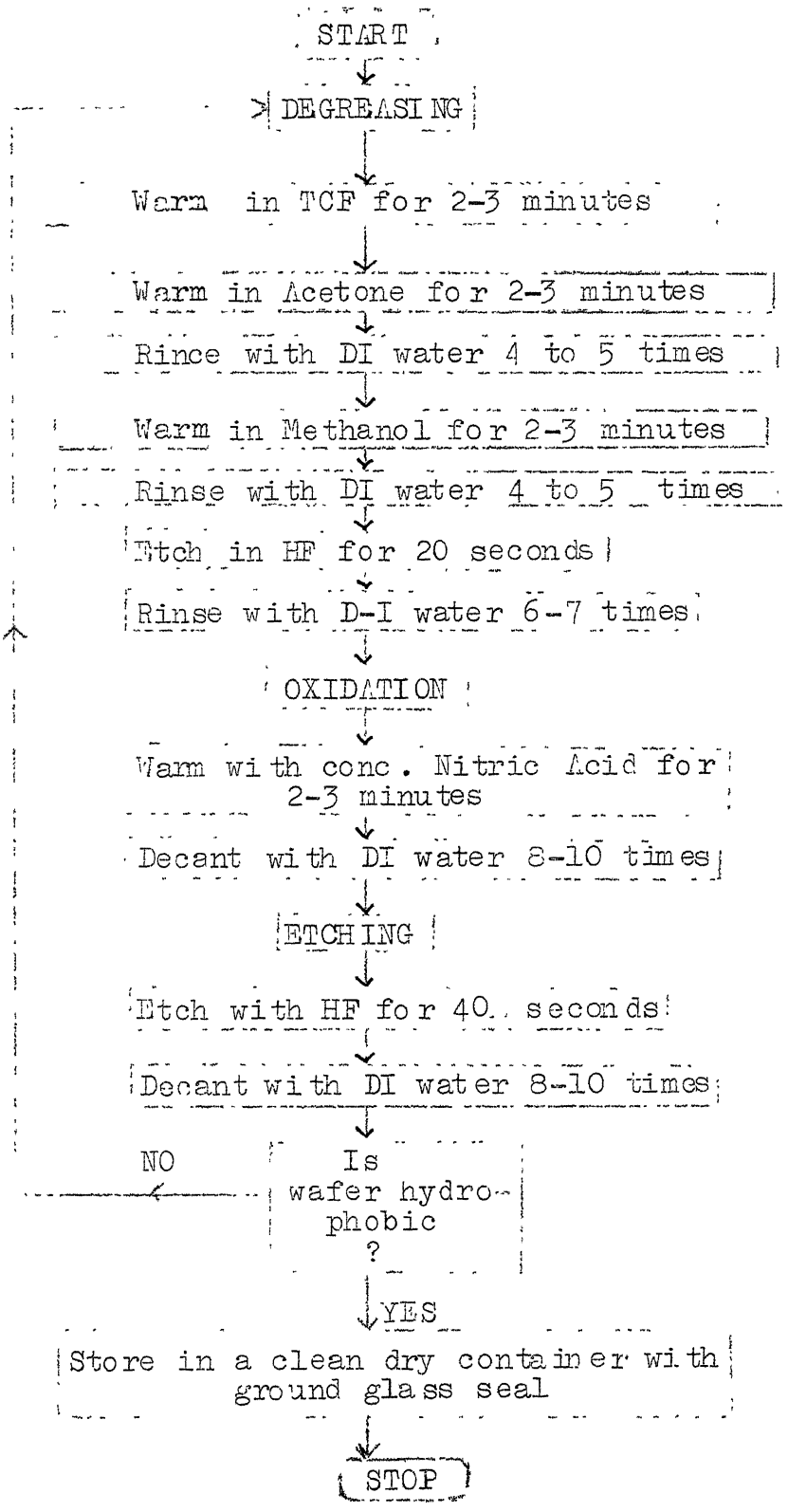


Fig. 2.1: Silicon Wafer Cleaning

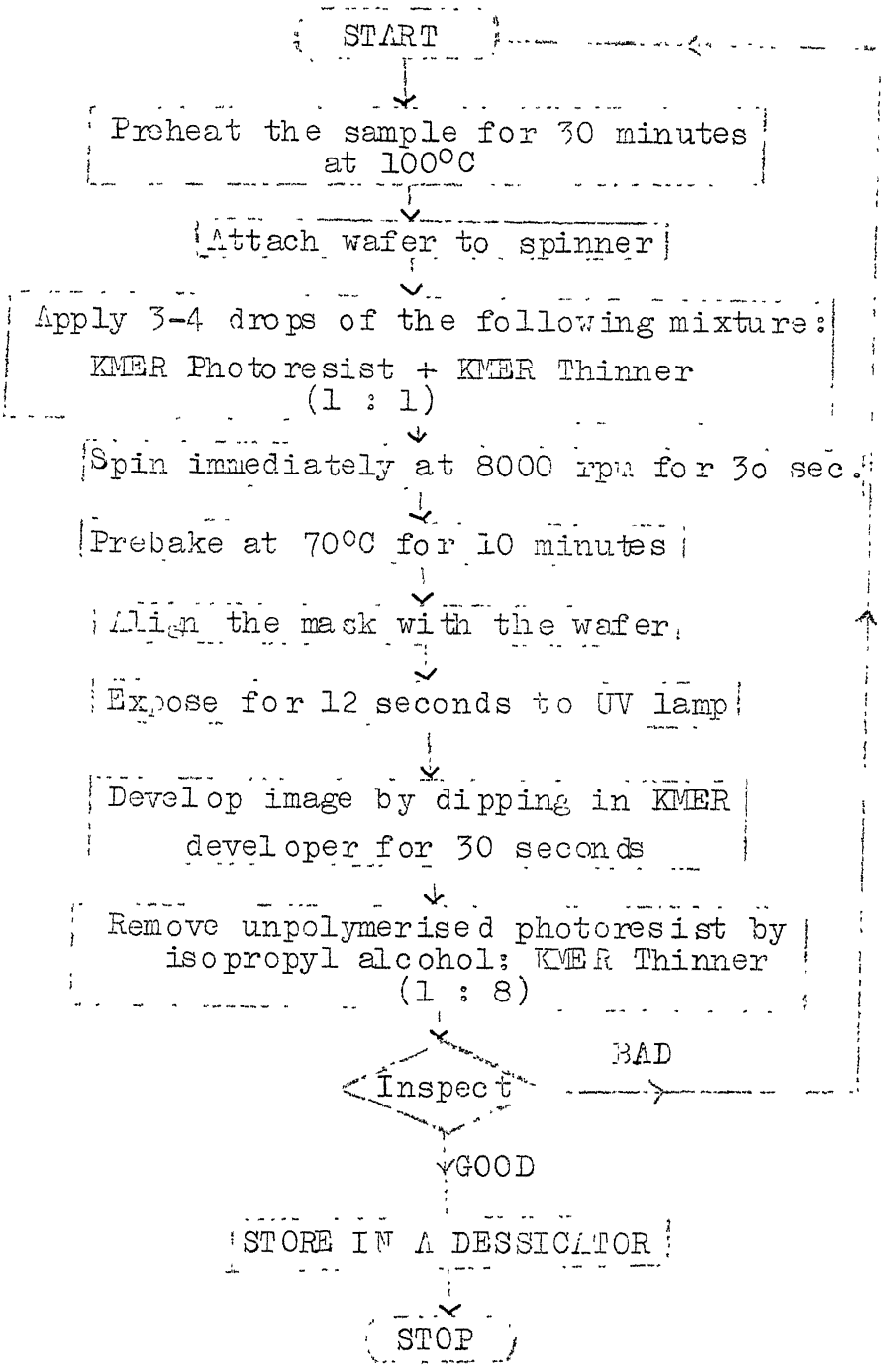
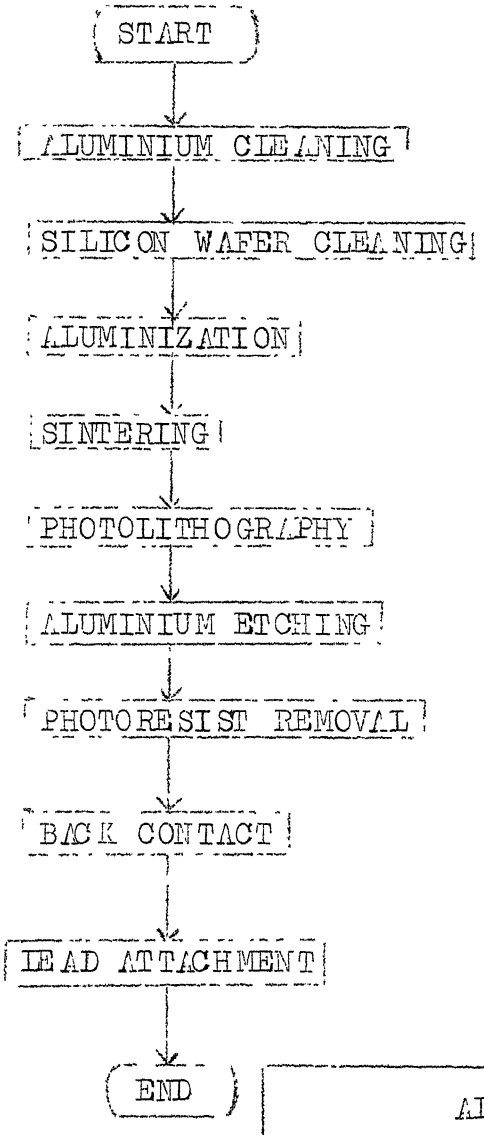


Fig. 2.2: Aluminium Photolithography.



ALUMINIUM ETCHANT

375 ml. Phosphoric acid (80)
15 ml. HNO_3 (70)
75 ml. Acetic acid (99)
70 ml. DI water
at 40°C rate of removal of aluminium (Solution 5-times diluted) 400 Å/min.

Fig. 2.3 : Device Fabrication Flow Chart.

Aluminium etching was a crucial step in the device fabrication. Previously very high rates of etching were tried ($\sim$250 Å/sec.). This, however, proved futile as during the rapid etching of the bare aluminium slight undercutting of the covered aluminium also took place. The attack from the sides on the photoresist covered aluminium, in some cases, was sufficient to etch aluminium from those regions also. This undercutting resulted in broken grid strips. This was minimised by diluting, the aluminium etchant about 5 times. This reduced the etch rate to about 400 Å/min. and the side attacks on the grid strips became less troublesome.

It was found that the heat treatment of the aluminised silicon wafer, in ultrapure argon, improved the adhesion of the Al-film significantly. The heat treatment causes rapid diffusion of silicon in the evaporated Al-film. This process is completed in about 15 minutes, for a temperature around 525°C [26]. Slow cooling of the sample starts the precipitation of silicon from aluminium. Subsequent the rate of precipitation depends upon the rate of cooling which was varied from 3°C/min. to 7°C/min. but no significant change in the ultimate device performance was observed. This heat treatment may also have affected the barrier height of the Al-Si system. But no definite clue to this increase in the barrier could be observed.

2.4 RESULTS:

The lateral SBSCs have been fabricated on n-type silicon wafers. The experiments were confined only to n-type wafers as these give scope for heat treatment (discussed in sec. 2.3), leading to better adhesion. A very good adhesion was required to avoid the peeling off of the film during Al-etching and photoresist removal. A p-type silicon could not be used, as any attempt of a meaningful heat treatment would make the Al-Si contact ohmic.

The grid structure used, as explained earlier, is not optimised for n-type silicon. The grid widths and grid spacings are 75 μm and 375 μm respectively, whereas the minority carrier diffusion length, in n-type Si-wafers is around 10 μm. This results in a huge loss of light generated carriers due to their recombination in the bulk semiconductor.

In the fabricated cell, the short circuit current is 2μ amp for an area of .5 cm^2 and the open circuit voltage 130 mV. Prior to photolithography, the Al-Si system, in this case was given a heat treatment, in presence of argon, at 550°C for 15 minutes and then cooled slowly at a rate of 5°C/min. The I-V characteristics, under illuminated and dark conditions, of the cell is shown in Fig. 2.4. The

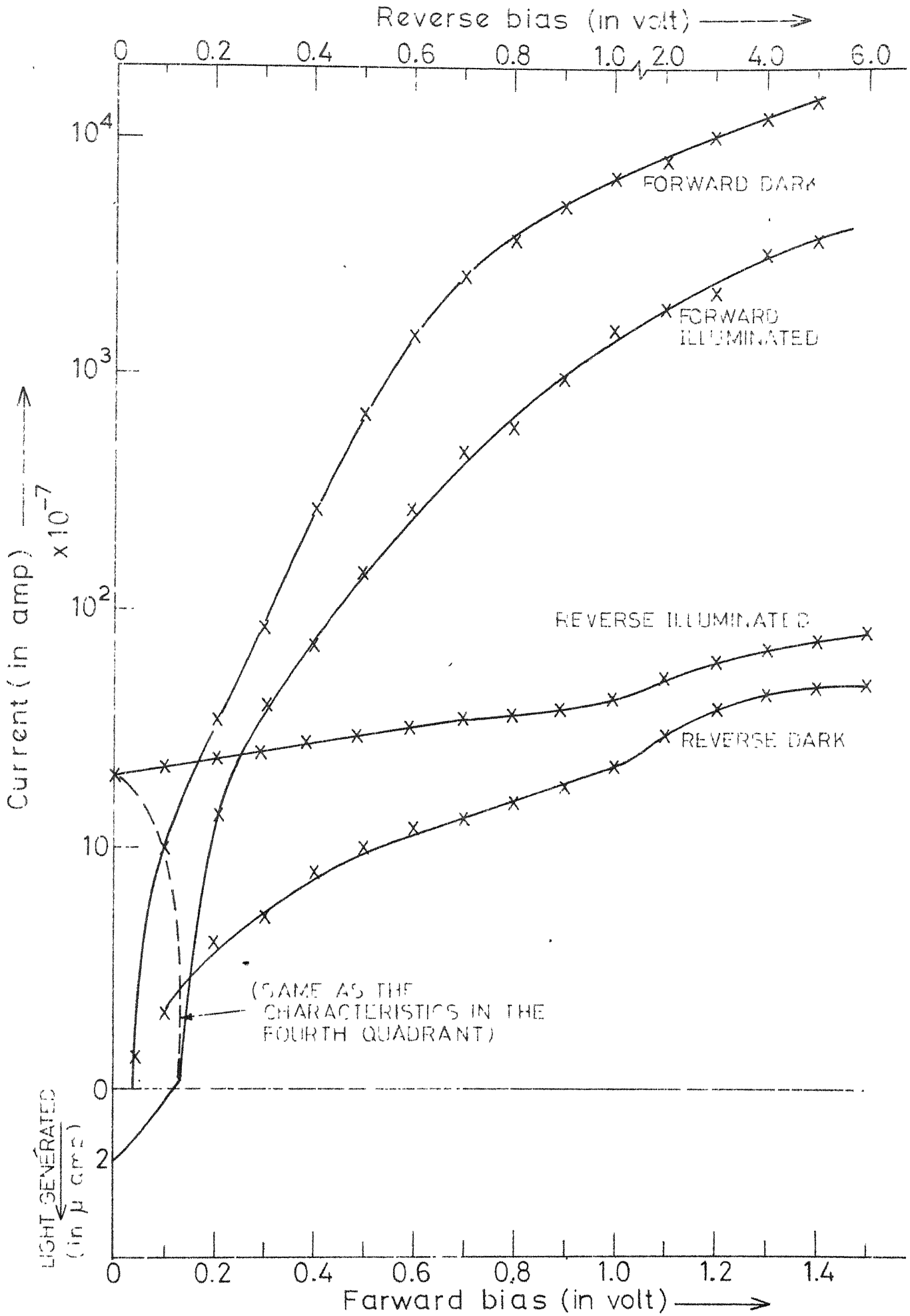


FIG. 2.4 EXPERIMENTAL CURVES

illuminated characteristics were taken under a tungsten lamp, standardised for sun's radiation.

An improvement in the performance of the cell is expected with an optimised grid structure.

CHAPTER III

DEVICE ANALYSIS

3.1 INTRODUCTION:

The present work is oriented towards the analysis of the structure described in sec. 1.7. A rigorous analysis of this structure using simultaneous solutions of Poisson, Continuity and Carrier transport equations, as shown in Fig. 3.1, is extremely complicated. However, a simulation, using lumped equivalent circuit model, gives a powerful way of analysis of such a system. Here, the junction is represented as a light generated current source and a diode, along with an appropriate series resistance. The model and the scheme is described, in detail, in the following sections. The details regarding the calculation of light generated current, collection efficiency, thermally generated carrier current and circuit simulation are discussed in sec. 3.2 and sec. 3.3 respectively. In sec. 3.4, the mode of calculations is mentioned. In sec. 3.5, analysis is done to yield device performance and its sensitivity to fabrication parameters such as grid width, grid spacing, series resistance of the cell etc. The effect of surface recombination on the ultimate conversion efficiency of the system is

MOST GENERAL APPROACH:

Simultaneous solutions of following equations:

A. Carrier transport eqns.:

$$\vec{J}_e = q\,\mu_n\, n\,\vec{E} + q\,D_n\vec{\nabla}_n$$

$$\vec{J}_h = q\,\mu_h\, p\,\vec{E} - q\,D_h\vec{\nabla}p$$

$$\vec{J}_{cond.} = \vec{J}_e + \vec{J}_h$$

B. Continuity eqns.:

$$\frac{\partial n}{\partial t} = G_e - U_e + \frac{1}{q}\vec{\nabla}.\,\vec{J}_e$$

$$\frac{\partial p}{\partial t} = G_h - U_h - \frac{1}{q}\vec{\nabla}.\,\vec{J}_h$$

C. Poisson eqn.:

$$\nabla^2 V = -\vec{\nabla}.\,E = -\frac{\rho(X)}{\varepsilon_s}$$

Here, the symbols have their usual meanings

Simplifying assumptions:

a) The photo generated carriers move along the direction of the incident radiation an the transport of excess carriers is governed by 1-dimensional diffusion eqns.

b) The structure is separated into regions with sharp boundaries i) space charge neutral region and ii) region fully depleted of mobile carriers

Equations are (i) 1-dimensional and (ii) decoupled

Poisson eqn.

$$\frac{d^2V}{dx^2} = -\frac{\partial E}{dx} = -\frac{\rho(x)}{\varepsilon_s}$$

C-V characteristics

Continuity equations

$$D_h\frac{d^2p}{dx^2} - \frac{p}{\tau_h} + G = 0$$

$$D_e\frac{d^2n}{dx^2} - \frac{n}{\tau_e} + G = 0$$

With appropriate boundary conditions of surface recombination velocity, junction geometry etc.

Algebraic addition of lumped sources (as is done in the present analysis)

Short circuit current

Fig. 3.1: Flow-Diagram for the Analysis.

also studied in this section. The conclusions are mentioned in sec. 3.6.

3.2 THEORETICAL MODELLING:

Theoretical investigations of solar cell performance require an understanding of photon absorption in the semiconductor, carrier generation by the absorbed photons, carrier collection in a given device structure, thermally stimulated junction currents and the circuit aspects such as series, shunt and loading resistances. However, in the present analysis, only those details that are necessary for arriving at the terminal I-V characteristics are considered.

A. Assumptions:

In the investigation, following assumptions are made:

(i) The reflectivity of the surface is zero.

(ii) The carriers are generated in the bulk semiconductor. Effects due to the surface recombinations are not considered. This assumption is later relaxed to study the effect of surface recombination on the ultimate conversion efficiency.

(iii) The quantum-efficiency is unity i.e. each absorbed photon of sufficient energy (i.e. energy greater than the bandgap of the semiconductor) produces one e-h pair.

(iv) Resistivity, and minority carrier life-times are constant within the substrate i.e. there exists no doping gradient in the substrate.

(v) The cell is uniformly illuminated. This allows the analysis of only one unit field (described later) and the addition of all such units in parallel gives the total cell performance.

(vi) The resistance of the grid and conductance strips is negligible.

There are other simplifying assumptions also, but they are made for the convenience in calculations. They can be relaxed and taken into account by a slightly complex approach. They are mentioned in the following sections, at appropriate places.

B. Light Generated Carriers:

A lumped circuit representation demands the knowledge of the distribution of light generated carriers in the entire device. This can be calculated as follows:

The number of photons absorbed per unit volume per sec. in a layer of thickness d_z is given by Lambert's Law,

$$n(\lambda)\, d_x = \alpha(\lambda)\, N(\lambda) \exp(-\alpha(\lambda) Z)\, d_x \qquad (3.1)$$

where, $\alpha(\lambda)$ is the absorption coefficient, $N(\lambda)$ is the number of incident photons per unit area per unit time in the interval λ to $\lambda + d_\lambda$. Assuming quantum efficiency to be unity, the total carriers generated as a function of depth (d) would be,

$$N(d) = \int_{0}^{d} \int_{\lambda_1}^{\lambda_G} \alpha(\lambda)\, N(\lambda) \exp\left(-\alpha(\lambda) Z\right) d_\lambda\, d_z \qquad (3.2)$$

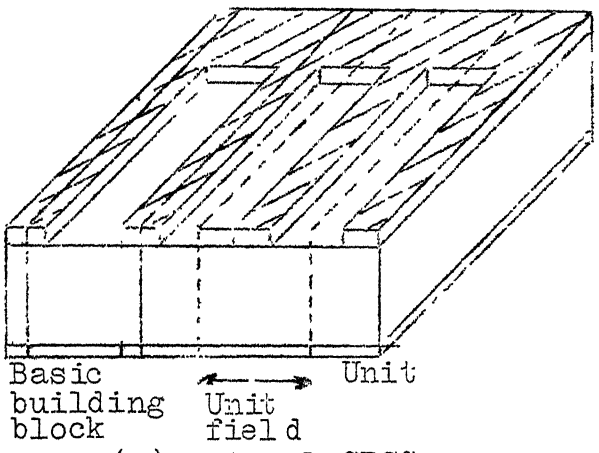
The integration limits for wavelength is determined by the absorption curve - upper limit being the minimum energy required for e-h pair creation and the lower limit determined by wavelengthfor which the absorption is too large to have significant absorption beyond the surface layer.

C. Carrier Collection:

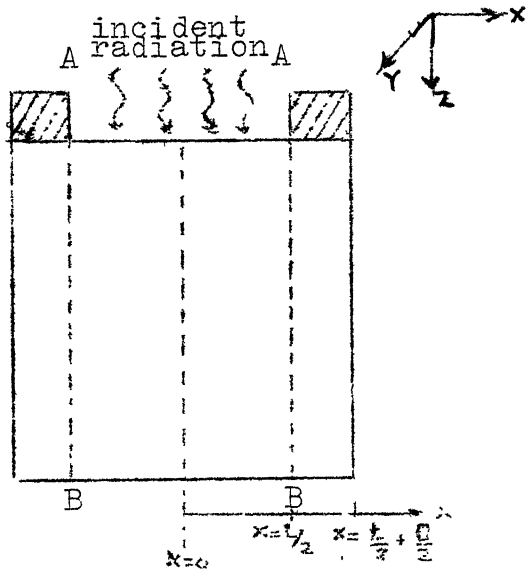
The shortcircuit current (I_{sc}), in a solar cell, is due to the minority carriers reaching the junction. However, all the light generated carriers donot reach the junction, as a part of it gets recombined. Therefore, the number of collected carriers is an important quantity that determines the short circuit current and, hence, the overall collection efficiency. A complete rigorous analysis of carrier collection should be carried out according to the flow-diagram given in Fig. 3.1. The problem may be simplified by making suitable approximations. A 1-dimensional analysis is done, in this section, to calculate short circuit current.

The structure, shown in Fig. 3.2(a), can be divided into two regions: illuminated and unilluminated, i.e. those regions which are exposed to the incident radiation and those which are covered by thick metallic grids. Now let us

consider the basic building block of the cell (shown in Fig. 3.2(a)).



(a) Lateral SBSC



(b) Side view of the basic building block

Fig. 3.2

Assuming that the incident radiation penetrates uniformly across the cross-section, the carriers produced near the middle of the illuminated region would tend to diffuse outwards. This diffusion is two dimensional in as much as it takes place in both x- and y- directions. But, we shall neglect the diffusion of carriers in y-direction. Therefore, we shall have to solve the continuity equation in x-direction only. Again, the illuminated region is symmetrical about $x = 0$ and, hence, the solution needs to be considered only for $x \geq 0$.

Let us assume the semiconductor to be p-type. The analysis is valid for n-type semiconductor also. The continuity equation in the illuminated region, may be written as,

$$D_n \frac{d^2 n_1}{dx^2} - \frac{n_1}{\tau_n} + g_{L1} = 0 \qquad 0 \leq x \leq L/2 \qquad (3.3)$$

Here, n is the excess concentration of minority carriers (electrons), D_n and τ_n are the diffusion constant and life time of the minority carriers respectively. g_{L1} is the number of light generated carriers per unit volume per sec. It is given by equation (3.1) which is reproduced below,

$$g_{L1} = N(\lambda)\, \alpha(\lambda) \exp(-\alpha(\lambda)\, z) \qquad (3.4)$$

Here quantum efficiency has been taken to be unity and reflection losses are neglected. The solution of equation (3.2) with proper boundary conditions is given in Appendix I. From this, the diffusion current density at the boundary AB would be (cf. Fig. 3.2)

$$J_{n1} \equiv J_{n1}(x)\Big|_{x=L/2} = q\, g_{L1}\, L_n \exp(-L/2L_n)x \times \text{Sin h}\, \frac{L}{2L_n} \qquad (3.5)$$

Now, let us consider the unilluminated region separately. In this region, the diffusion in x-direction is neglected because the 'width' of this region is very small. Thus, the carriers that diffuse laterally to the boundary AB (from the illuminated region), in turn, would diffuse in the vertically upward direction to the metal-

semiconductor junction (MS junction). We consider a parellelopiped of unit cross-sectional area and length B/2 in the unilluminated region (Fig. 3.3), and assume that the number of carriers entering the parellelopiped per unit volume per sec. are $J_{n1}/(q.B/2)$, where J_{n1} is a function of z, as is evident from eqns. (3.5) and (3.4).

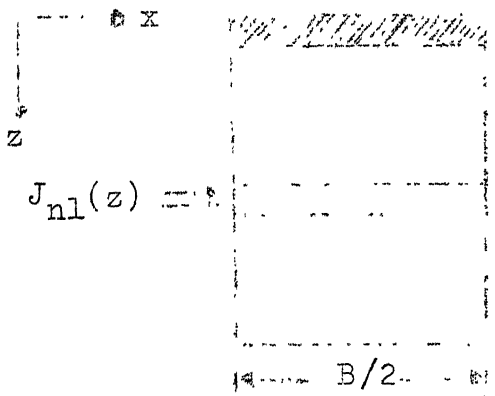


Fig.3.3 Unilluminated region

The continuity equation in this region may be written as,

$$D_n \frac{d_{n2}^2}{d_z^2} - \frac{n_2}{\tau_n} + g_{L2}(z) = 0 \qquad (3.6)$$

where,

$$g_{L2}(z) \equiv \frac{J_{n1}(z)}{q.B/2} = \frac{g_{L1}(\lambda,z)\, L_n\, e^{-L/2L_n}\, \text{Sin h}(L/2L_n)}{B/2} \qquad (3.7)$$

$g_{L1}(\lambda,z)$ is given by eqn. (3.4). This equation, along with, proper boundary conditions, is solved in Appendix II. The boundary conditions are,

$$\text{at } z = 0, \quad n_2 = 0$$
$$\text{at } z = \infty, \quad \frac{d_{n2}}{d_z} = 0 \tag{3.8}$$

The diffusion current density J_{n2} in this region would be given by,

$$J_{n2}(z) = q D_n \frac{d_{n2}}{d_z} = \frac{\chi [\alpha e^{-\alpha z} - \frac{1}{L} e^{-z/L_n}]}{DB/2} \tag{3.9}$$

where,

$$\chi = L_n N(\lambda) \alpha(\lambda) \text{ Sin h}(L/2L_n) . e^{-L/2L_n} \tag{3.10}$$

At the MS junction,

$$J_{n2} \equiv J_{n2}(z) \Big|_{z=0} = \frac{\chi}{B/2(\alpha + 1/L)D} \tag{3.11}$$

The same value of J_{n2} could be arrived at if the carrier generation term $g_{L2}(\lambda,z)$ is multiplied by $e^{-z/L}$ (to take care of bulk-recombination) and is integrated over the whole range of z(i.e. 0 to ∞).

Therefore,

$$J_{n2} = \frac{\chi}{D(\alpha + 1/L)B/2} = \int_0^\infty \frac{J_{n1}}{B/2} \cdot e^{-z/L_n} d_z \tag{3.14}$$

Hence, the short circuit current density J_{sc} overall wave lengt may be written as,

$$J_{sc} = \int_{\lambda_1}^{\lambda_G} J_{n2}(\lambda)\, d\lambda = \int_{\lambda_1}^{\lambda_G} d\lambda \int_{0}^{\infty} \frac{J_{n1}}{B/2} \cdot e^{-z/L_n} dz \quad (3.15)$$

where λ_1 and λ_G limits have been obtained earlier.

For simplicity in calculations, we make two approximations: (i) only the carriers that are generated with in a diffusion length from the MS junction are collected by the junction, (ii) the illuminated portion can be divided into six regions, so as to contribute approximately the same numbers of generated carriers in each of them. This is shown in Fig. 3.4 for an unit field.

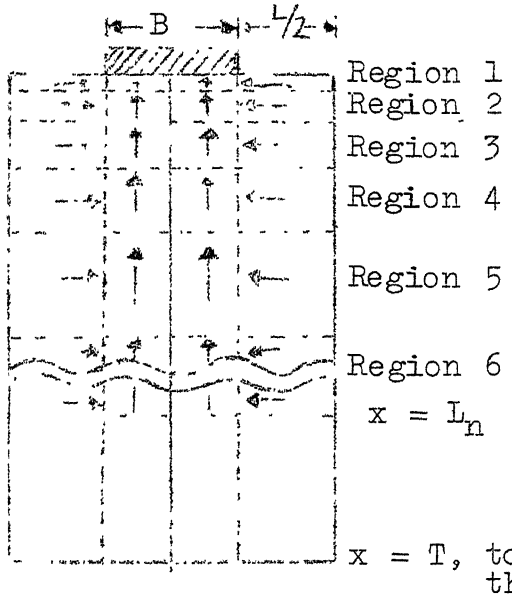


Fig.3.4: Configuration of an unit field.

The depth of each junction and number of carriers generated are given in Table 1 [27].

From the above two assumptions, the integration in eqn. (3.15) may be replaced by summation over the six regions.

Table 1: Configuration of an unit field.

Region	No. of Carriers (N) (per cm^2 per sec.)	Range
1	10^{17}	0 - 1 μ
2	5×10^{16}	1 - 2 μ
3	5×10^{16}	2 - 4 μ
4	5×10^{16}	4 -10 μ
5	5×10^{16}	10 -40 μ
6	3×10^{16}	40-100 μ

Hence, I_{sc} would be,

$$I_{sc} = \int_{\lambda_1}^{\lambda_G} d_\lambda \sum_{i=1}^{6} J_{nl_i}(\lambda)\, e^{-d_i/L_n} \qquad (3.16)$$

where, J_{nl_i} is the contribution to J_{nl} from the i-th region, d_i is the mean depth of the i-th region.

D. Reverse Saturation Current:

In addition to generation due to incident radiation, minority carriers are also generated due to thermal excitation. This results in a reverse saturation current, which determines the open circuit voltage V_{oc} (cf. equation 1.4), I_o can be evaluated using standard junction equation (1.3) reproduced below

$$I_o = A^* T^2 e^{-q\varphi_B/kT}$$

Various materials and structural parameters used for simulation are given in Table 2.

Table 2: Simulation parameters (material-silicon)

Cell dimension	1 cm x 1.1 cm x 300 μm
Width of the contact strip	.1 cm
Thickness of the grid and contact-strip	10,000 Å
Minority carrier diffusion length (L_n)	100 μm
Resistivity of the semiconductor (ρ)	1 ohm . cm
Intrinsic carrier concentration (n_i^2)	$2.5 \times 10^{20}/cm^6$
Effective radiation flux (over .3-1.5 μm spectral width)	100 m Watts/cm^2

3.3 CIRCUIT SIMULATION:

The equivalent circuit of the unit field with two junctions is developed in this section. A parallel combination of these unit fields give the overall cell performance.

The simulation takes into account the effect of decreased reverse saturation current due to decreased junction area, series resistance due to grid strips, contact resistance etc. and circuit conditions such as loading. The circuit model for a unit field, shown in Fig. 3.5, is derived from the current flow in lateral SBSC. The currents

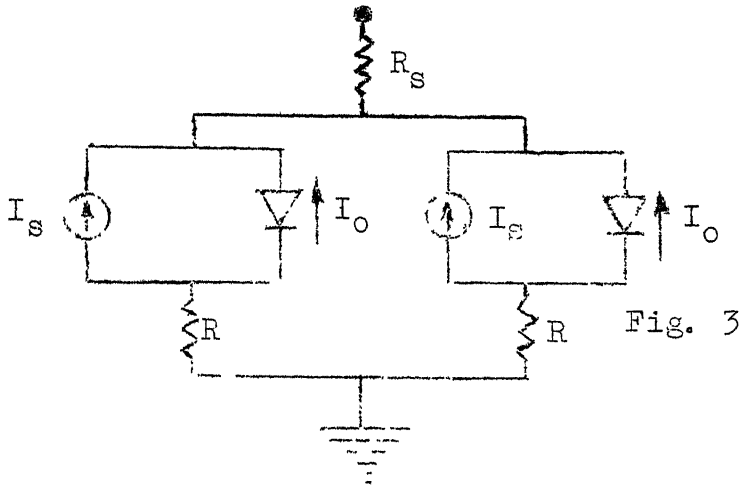


Fig. 3.5: Circuit mode for an unit field.

due to collected light generated and thermally generated carriers can be determined for various device conditions discussed in previous section. The model can be easily modified to include the role of surface recombination, as is done in Sec. 3.5. The resistance R arises due to the resistance faced by the carriers in the bulk semiconductor, whereas R_s is due to the sheet resistance of the grid strips and the contact resistance. R_s, however, is presently assumed to be zero.

To get the I-V characteristics of the whole cell, the individual I-V characteristics of each unit should be obtained. This problem is non-linear because of the presence of a diode. The most general method to solve such type of nonlinear problems is to use Computer Aided Design (CAD) techniques. In this technique, the nonlinear diode is

replaced by its linear equivalent and the nodal equations for the circuit are formed. These equations are then solved, on computer, using iterative techniques. Since, the present problem is comparatively simpler, it is solved by using the technique of graphical analysis. The equivalent model of a cell having n unit fields (or n grid strips) is shown in Fig. 3.6.

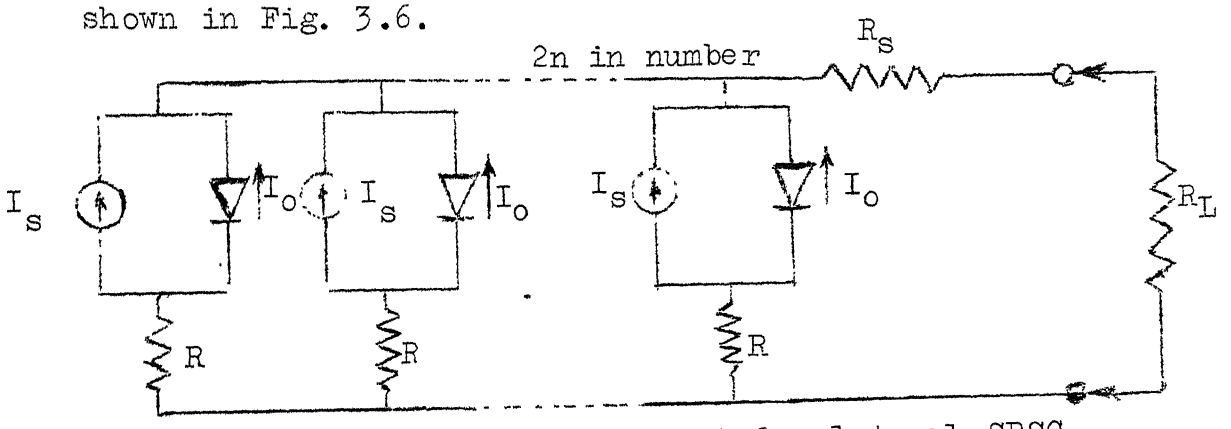


Fig.3.6: Equivalent circuit for lateral SBSC.

Since the individual unit fields are identical in all respects, the total I-V characteristics of the cell can be derived from the I-V characteristics of an individual unit by multiplying it appropriately by the total number of units.

3.4 CALCULATIONS:

The I-V characteristics of the circuit shown in Fig. 3.7 can be expressed as follows:

$$I = I_s - I_D \tag{3.17}$$

or,

$$I = I_s - I_o \left(e^{qV_D/nkT} - 1\right) \tag{3.18}$$

i.e.

$$V_D = \frac{nkT}{q} \ln \left(\frac{I_s - I}{I_o} + 1\right) \tag{3.19}$$

therefore,

$$V = \frac{nkT}{q} \ln \left(\frac{I_s - I}{I_o} + 1\right) - IR \tag{3.20}$$

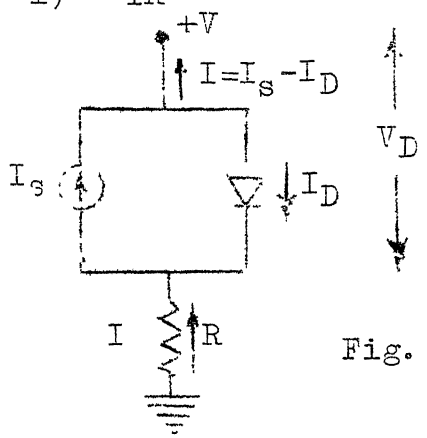


Fig. 3.7

Equation (3.20) is a non-linear equation thatis to be solved to get the I-V characteristics of the circuit shown in Fig. 3.7. The equivalent circuit shown of an unit field shown in Fig. 3.5 consists of a parallel combination of two circuits shown in Fig. 3.7 (excluding the series resistance R_s that is lumped, later, in the series resistance of the total cell). Therefore, the I-V characteristics of the unit field can be obtained by multiplying the current by a factor of two at each voltage V. As mentioned earlier, the overall I-V characteristics of the cell are obtained by

multiplying it by the number of unit cells and then taking the effect of series resistance R_s into account.

3.5 SIMULATION RESULTS:

The calculations have been directed towards the specific questions regarding the perfo mance dependence of some of the fabrication and technology parameters such as the ideality factor (n), the barrier height (φ_B), the surface recombination, the series resistance (R_s), the grid width (B) and the grid spacing (L) etc. The effect of contact resistance and the resistance of the grid has not been included in the present analysis, though it may be suitably lumped in the series resistance (R_s). These factors will reduce the short circuit current (I_{sc}) and overall conversion efficiency (η) of the cell.

(a) Ideality Factor Variation:

The ideality factor 'n' (described in sec. 1.4) depends on various factors like surface states, interfacial layer etc. Its value can be determined from the slope of the forward I-V characteristics of the cell. The cell, with different 'n' values, was simulated. The results are shown in Fig. 3.8. It can be inferred that 'n' does not appreciably alter I_{sc} but affects open circuit voltage (V_{oc}) significantly. A typical value of 'n' for SBSCs is aroud 2.0 [16].

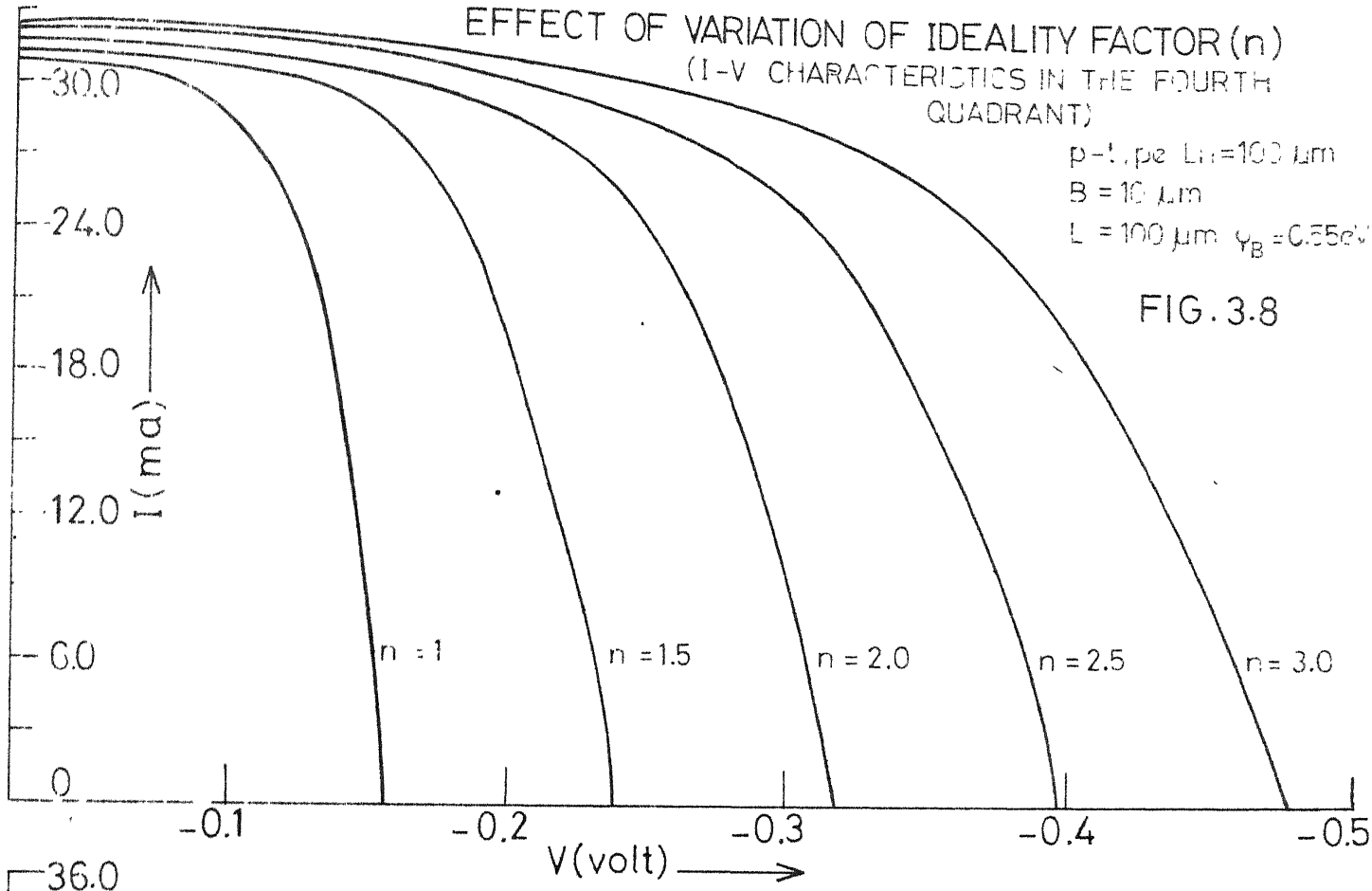

EFFECT OF VARIATION OF IDEALITY FACTOR (n)
(I-V CHARACTERISTICS IN THE FOURTH QUADRANT)
p-type Ln=100 μm
B = 10 μm
L = 100 μm ψB = 0.55eV
30.0
24.0
18.0
12.0
6.0
0
I (ma)
n = 1
n = 1.5
n = 2.0
n = 2.5
n = 3.0
-0.1
-0.2
-0.3
-0.4
-0.5
V(volt)

FIG. 3.8

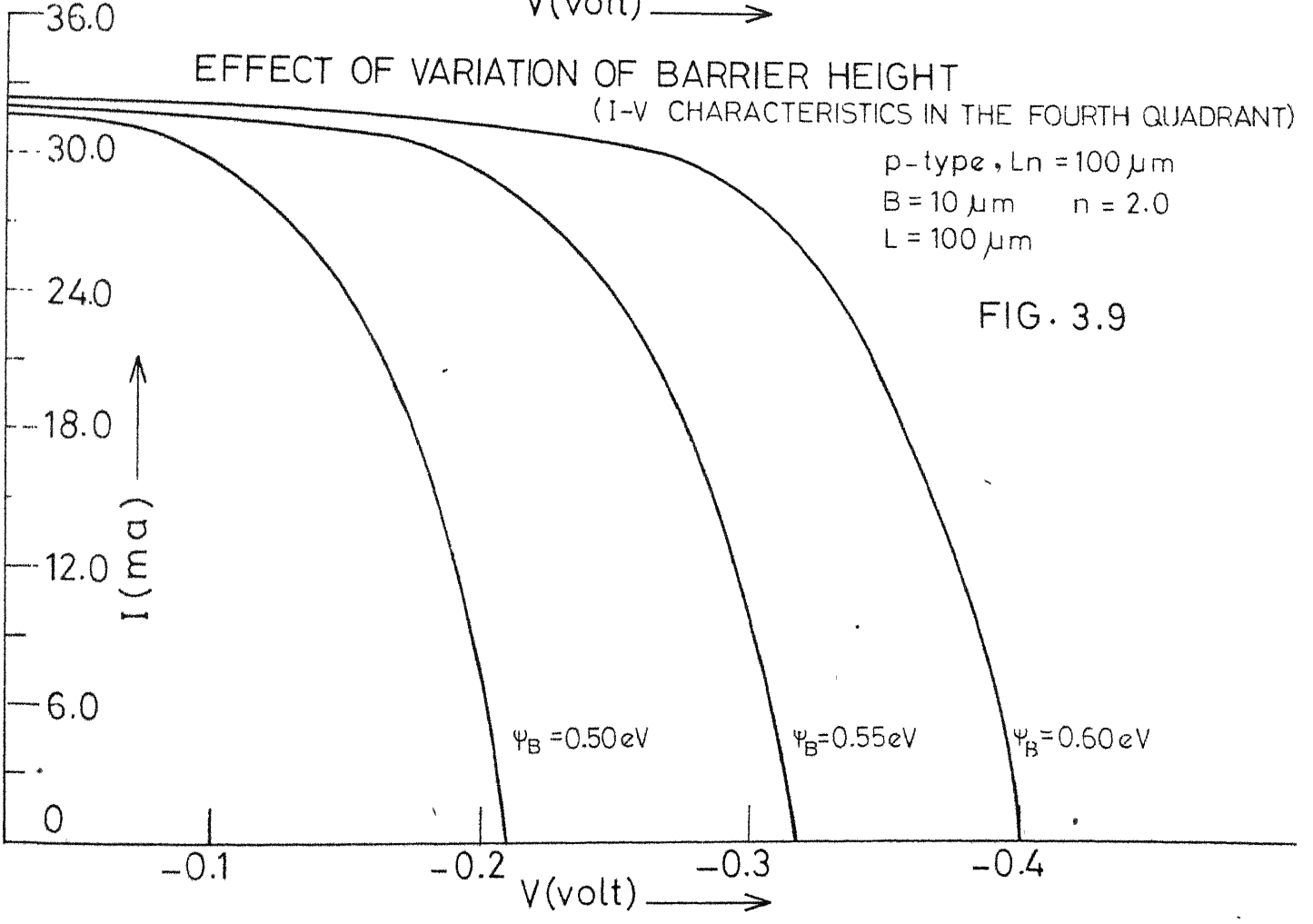

36.0
EFFECT OF VARIATION OF BARRIER HEIGHT
(I-V CHARACTERISTICS IN THE FOURTH QUADRANT)
p-type, Ln = 100 μm
B = 10 μm n = 2.0
L = 100 μm
30.0
24.0
18.0
12.0
6.0
0
I (ma)
ψB = 0.50eV
ψB = 0.55eV
ψB = 0.60eV
-0.1
-0.2
-0.3
-0.4
V(volt)

FIG. 3.9

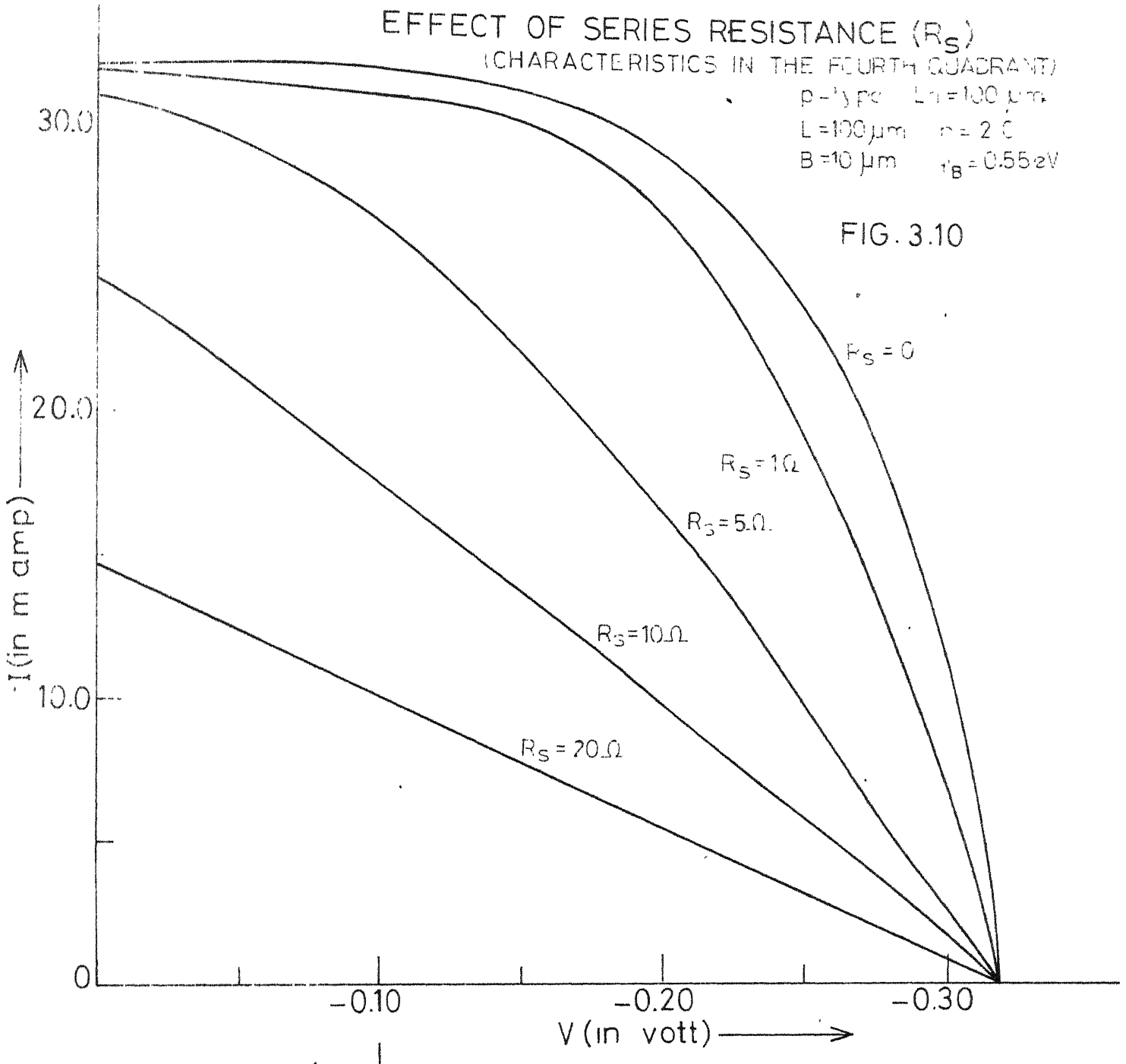


FIG. 3.10

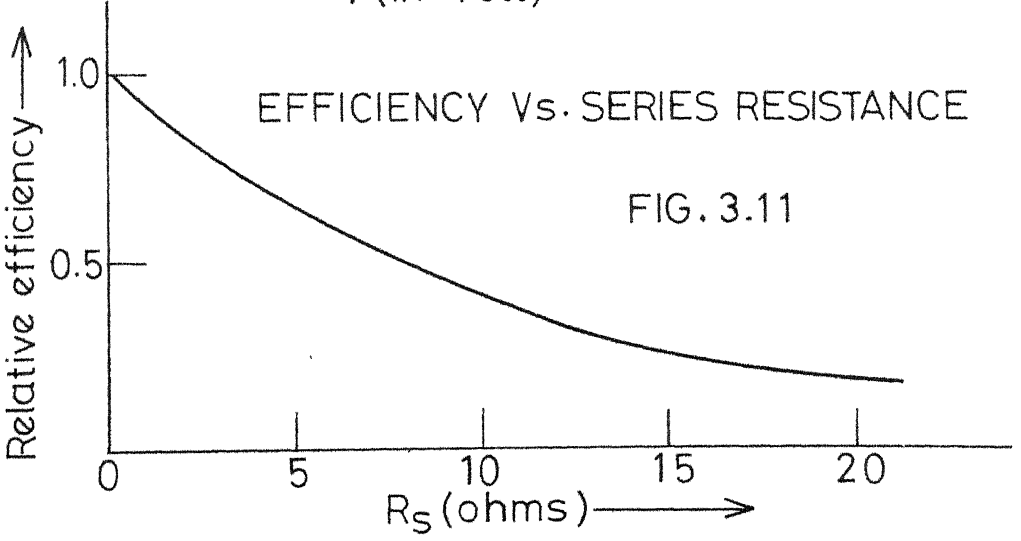


FIG. 3.11

(b) Barrier Height Variation:

The barrier height (φ_B) of the Al-Si system controls the reverse saturation current (I_o), which, in turn, controls V_{oc}. Its effect on the performance of the cell is shown in Fig. 3.9. As expected, with a variation in φ_B, V_{oc} is altered significantly while I_{sc} is only marginally affected. A typical value of 'φ_B' for Al-Si (p-type) system is around .55 eV - .57 eV.

(c) Effect of Series Resistance:

The series resistance (R_s) of the cell affects the fill factor and, hence, the ultimate conversion efficiency. Fig. 3.10 shows the effect of R_s on the performance of the cell. As can be inferred, even a small value of R_s alters the available energy significantly. A plot of relative conversion efficiency vs. R_s is shown in Fig. 3.11. This, when compared with the corresponding data for conventional SBSC (given in sec. 1.4), shows that the effect of R_s is less drastic in lateral SBSC. This is due to lesser light generated current in the case of lateral SBSC.

(d) L/B Ratio Variation:

M.A. Green [25] has calculated the efficiency of the lateral SBSC for various values of L/B ratio. In his calculations, no account of recombination of the light generated

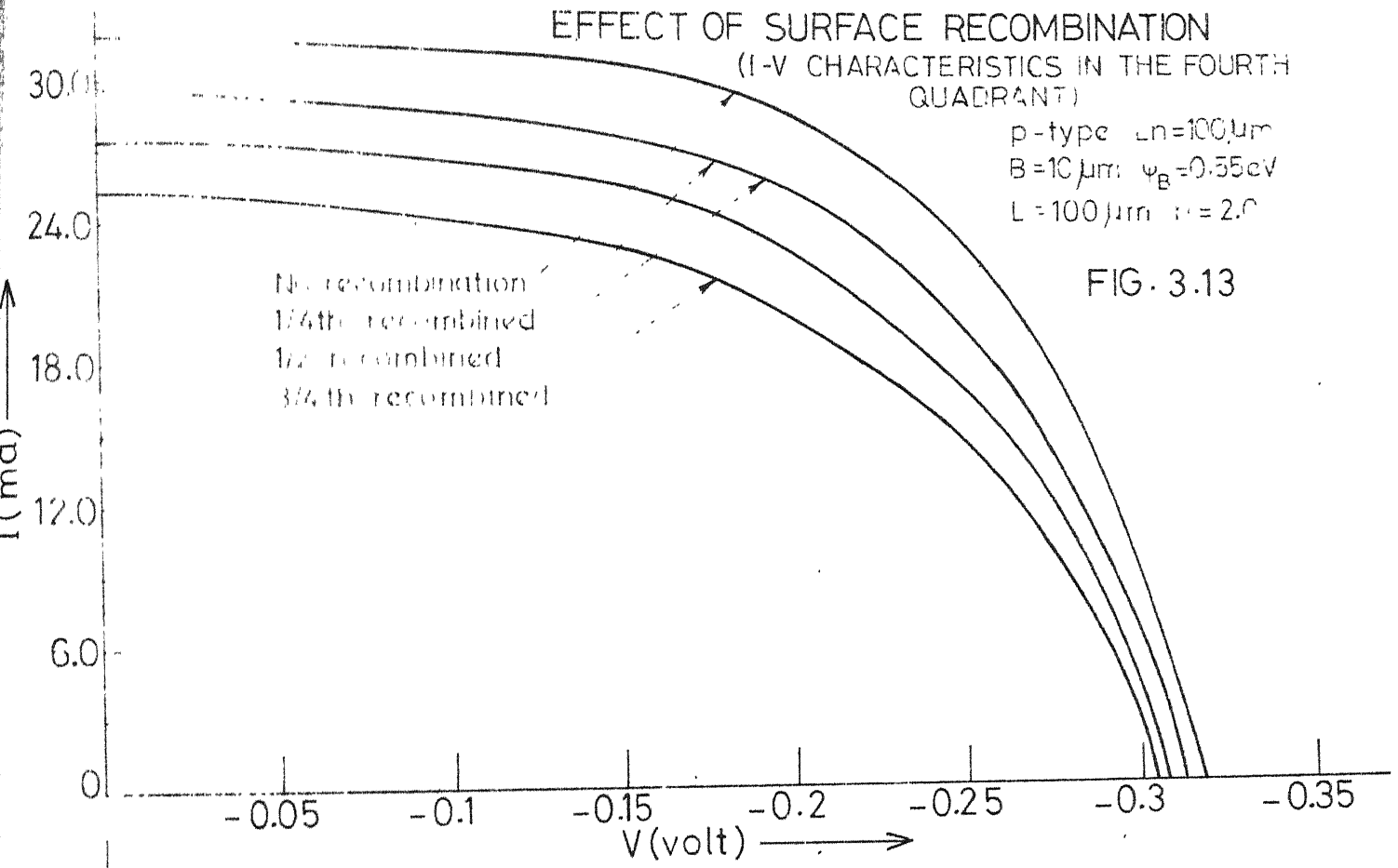


FIG. 3.13

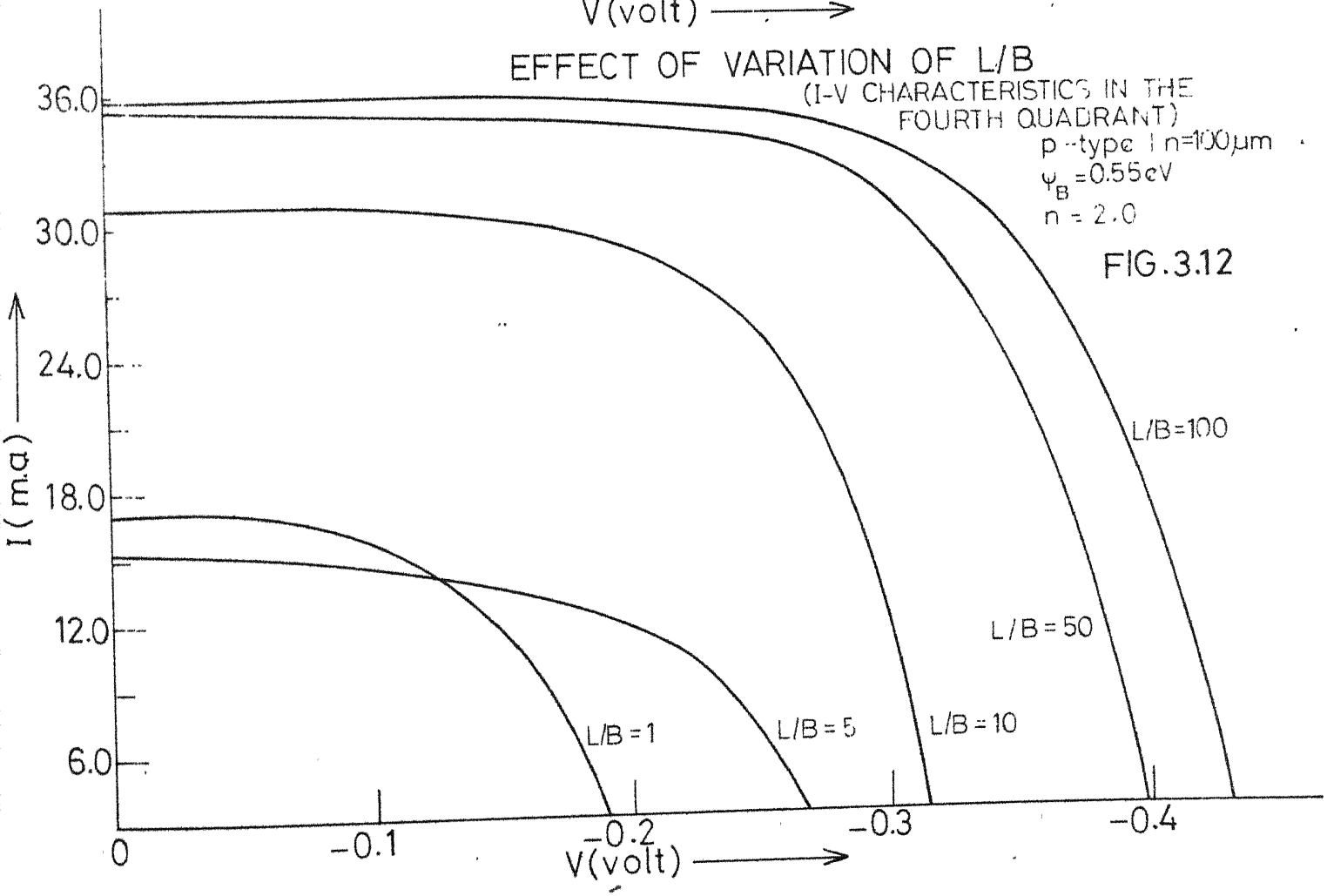


FIG. 3.12

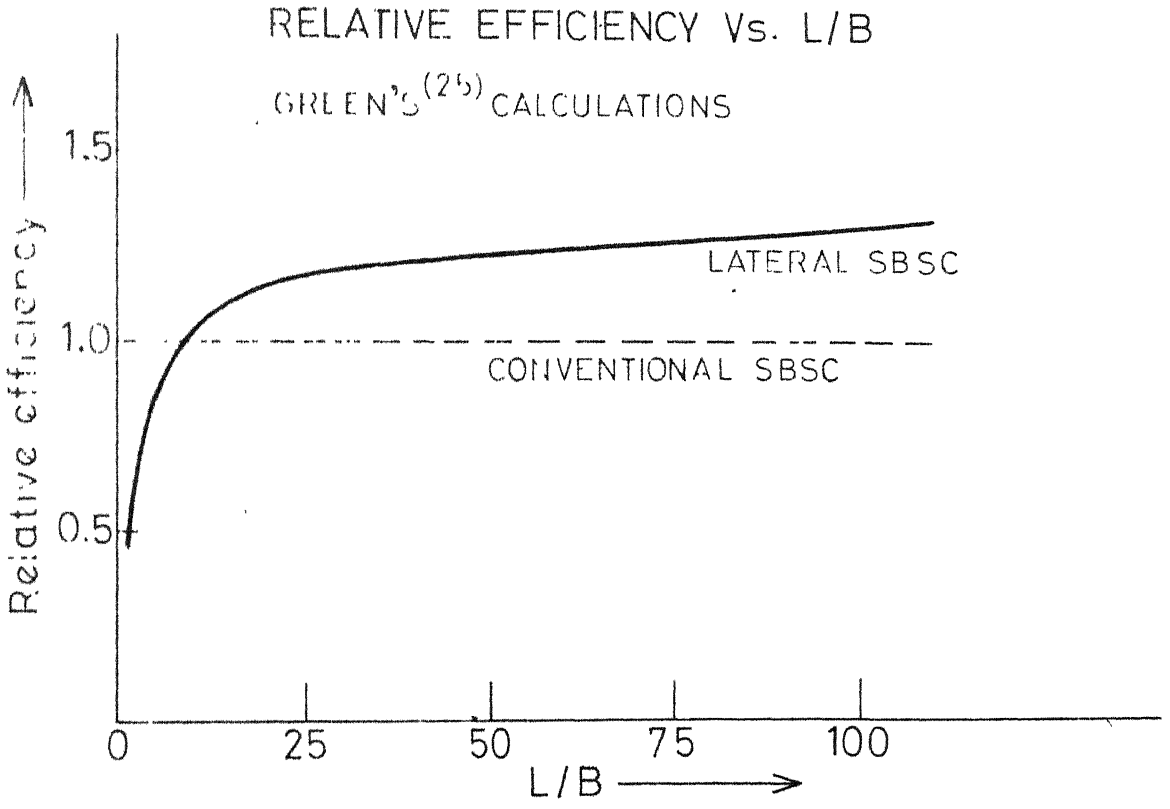


FIG. 3.14

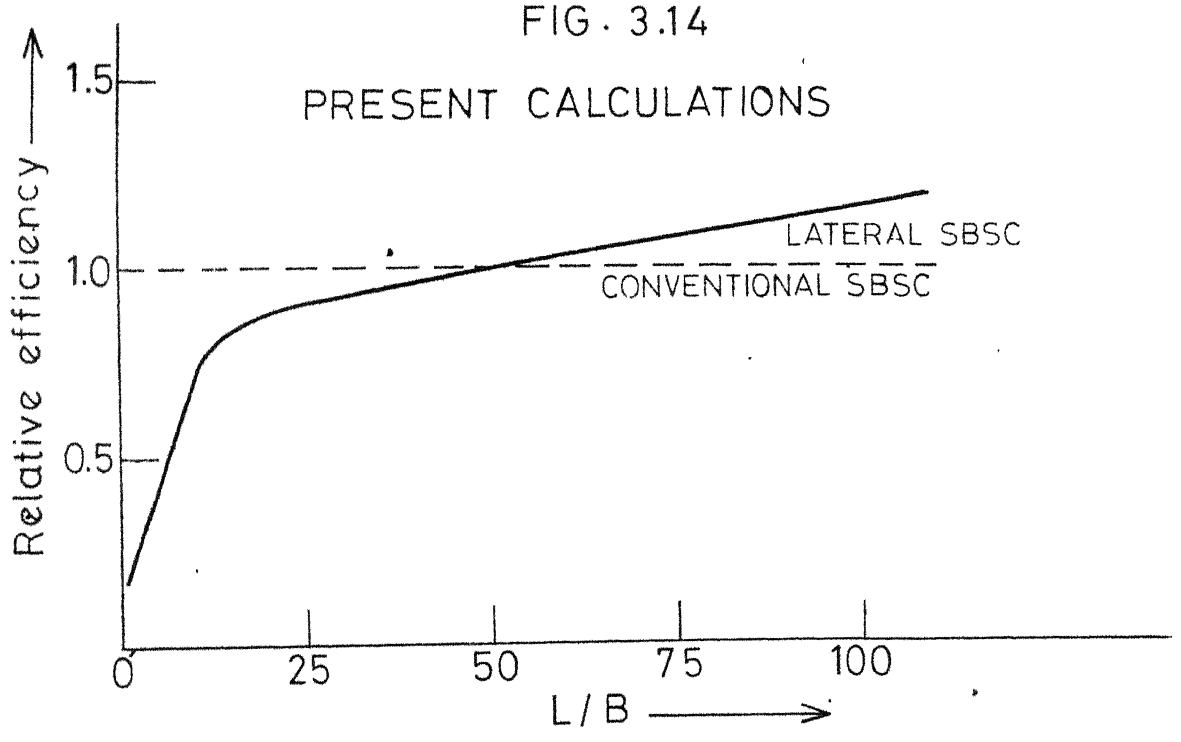


FIG. 3.15

carriers prior to their separation by the Metal-Semiconductor junction (MS junction) has been taken. A plot of relative conversion efficiency and L/B ratio, according to his calculations, is given in Fig. (3.14). However, in the present calculations, a first order account of carrier recombination has been taken. This lowers the efficiency of the cell. The performance of the cell for various values of L/B ratio is shown in Fig. (3.12). From this, the relative conversion efficiency (relative to conventional SBSC) of cells with different L/B ratio has been calculated. A plot of it is shown in Fig. (3.15).

A comparison of Fig. (3.14) and (3.15) shows that due to the recombination of the light generated carriers, the conversion efficiency of the lateral SBSC goes down. Furthermore, the efficiency of lateral SBSC is enhanced over that of the conventional SBSC, for a ratio L/B greater than 54 not 8 as shown by Green.

(e) Effect of Surface Recombination:

Surface recombination becomes crucial in lateral SBSC, as in this case, the carrier that are generated very near the exposed surface of the semiconductor reach the MS junction, depending upon the extent of surface recombination. In the present calculations, the surface recombination has been taken into accountby subjecting the carriers generated in region I

(cf. Table 1) to different degrees of recombination. This is because region I is only till 1 μm below the surface. Fig.3.12 shows the effect of various degrees of surface recombination on the performance of the cell. Here, the short circuit current is significantly effected. This calls for very well polished silicon surface.

3.6 SUMMARY AND DISCUSSION :

(1) A scheme is developed to analyse the lateral SBSCs. The scheme analyses effects of the grid structure, reduced junction area, bulk resistance, surface recombination etc.

(2) The simulation scheme requires light generated and thermally generated carriers and their current contributions as inputs.

(3) Light generated carrier distribution is determined from the solution of continuity equations in the illuminated and unilluminated regions of the cell. The boundary conditions are determined from the physical constraints and symmetry of the problem.

(4) The simulation results of the cell with different n and φ_B values are plotted. Both of them are found to affect V_{oc}, while I_{sc} remains comparatively unaffected.

(5) The influence of series resistance on the performance of the cell is found to be less drastic than that in the case of conventional SBSCs. This is attributed to lower light generated current involved in lateral SBSC.

(6) A study of variation in the performance of the cell with different L/B ratios ismade. Calculations are also done to find the relative conversion efficiency of the cell with different L/B values and, then, these are compared with that of the conventional SBSC. A similar calculations were done by M.A.Green [25]. A comparison shows that the recombination in the bulk semiconductor reduces the ultimate conversion efficiency of the lateral SBSC.

The major differences in the predicted efficiency of the first order models and a rigorous analysis (as shown in Fig. 3.1) may be an over-estimation of the minority carrier collection depth of the first-order model and an under-estimation of the recombination in the bulk semiconductor. The former can be taken care of by looking for the spatial point at which the minority carrier current in the base layer changes sign. This must represent the effective depth to which the carriers are collected. The recombination may be more effectively studied by solving 2-dimensional continuity equations in the illuminated and unilluminated region.

5.7 ANTIREFLECTION COATING:

In lateral SBSC, radiation is incident directly on the semiconductor surface. A part of the incident radiation is lost because of its reflection from the surface. This loss can be minimised by using an antireflection coating (ARC) of proper thickness. Materials generally used for antireflection coating, in case of silicon, are silicon mono-oxide, zinc sulphide, magnesium fluoride etc. The optimum thickness of the ARC is determined by the optical constants of the semiconductor and the coating material.

In this section, the variation in the transmission into the semiconductor, with wavelength of the incident radiation and thickness of the ARC, is studied. The calculations have been done with a computer program on IBM 7044. The systems investigated are ZnS-Si and SiO-Si.

A. Calculations:

This system may be considered as the case of an absorbing (in some part of the incident radiation spectrum) film on an absorbing substrate. The equations for calculating reflectance and transmittance of such a system has been given by Heavens [28]. The equations are given below for convenience:

$$g_1 = \frac{n_0^2 - n_1^2 - K_1^2}{(n_0 + n_1)^2 + K_1^2}$$

$$g_2 = \frac{n_1^2 - n_2^2 + K_1^2 - K_2^2}{(n_1 + n_2)^2 + (K_1 + K_2)^2}$$

$$h_1 = (2n_0K_1)/[(n_0 + n_1)^2 + K_1^2]$$

$$h_2 = 2(n_1K_2 - n_2K_1)/[(n_1 + n_2)^2 + (K_1 + K_2)^2]$$

$$C = 2(g_1g_2 - h_1h_2)$$

$$D = 2(g_1h_2 + g_2h_1)$$

$$\alpha_1 = (2\pi K_1 d_1)/(\lambda \times 10^4)$$

$$\gamma_1 = (2\pi n_1 d_1)/(\lambda \times 10^4)$$

$$P_2 = e^{\alpha_1} \text{ Cos } \gamma_1$$

$$q_2 = e^{\alpha_1} \text{ Sin } \gamma_1$$

$$t_2 = e^{-\alpha_1} (g_2 \text{ Cos } \gamma_1 + h_2 \text{ Sin } \gamma_1)$$

$$u_2 = e^{-\alpha_1} (h_2 \text{ Cos } \gamma_1 - g_2 \text{ Sin } \gamma_1)$$

$$p_{12} = p_2 + g_1t_2 - h_1u_2$$

$$q_{12} = q_2 + h_1t_2 + g_1u_2$$

$$t_{12} = t_2 + g_1p_2 - h_1q_2$$

$$u_{12} = u_2 + h_1p_2 + g_1q_2$$

$$R_{12} = (h_{12}^2 + u_{12}^2)/(p_{12}^2 + q_{12}^2)$$

$$Tr = \frac{n_2}{n_0} \cdot \frac{[(1+g_1)^2 + h_1^2][(1+g_2)^2+h_2^2]}{[e^{2\alpha_1}+(g_1^2+h_1^2)(g_2^2+h_2^2)\, e^{-2\alpha_1}+C \cos 2\gamma_1+D \sin 2\gamma_1]}$$

Here, n_0, n_1, n_2 are the refractive indices of air, ARC and silicon respectively and K_1, K_2 are the extinction coefficients of Silicon and ARC respectively. Data for n_1, n_2, K_1, K_2 for various wavelengths is given in Tables 3, 4 and 5. RFL and TRI are total reflection from ARC and total transmission to semiconductor respectively. Other parameters are defined merely for the sake of simplicity in calculations.

Here, two simplifying assumptions are made:

(i) The radiation is incident normally on the ARC.

(ii) The semiconductor is thick enough to absorb all the incident radiation. Therefore, no radiation reaches the back contact metal and, thus, does not affect the optical behaviour.

3. Results and Discussion:

(i) ZnS - Si System:

Transmission (Tr) versus wavelength (λ) of the incident radiation, with thickness (d) of the ARC has been plotted in Fig. 3.16.

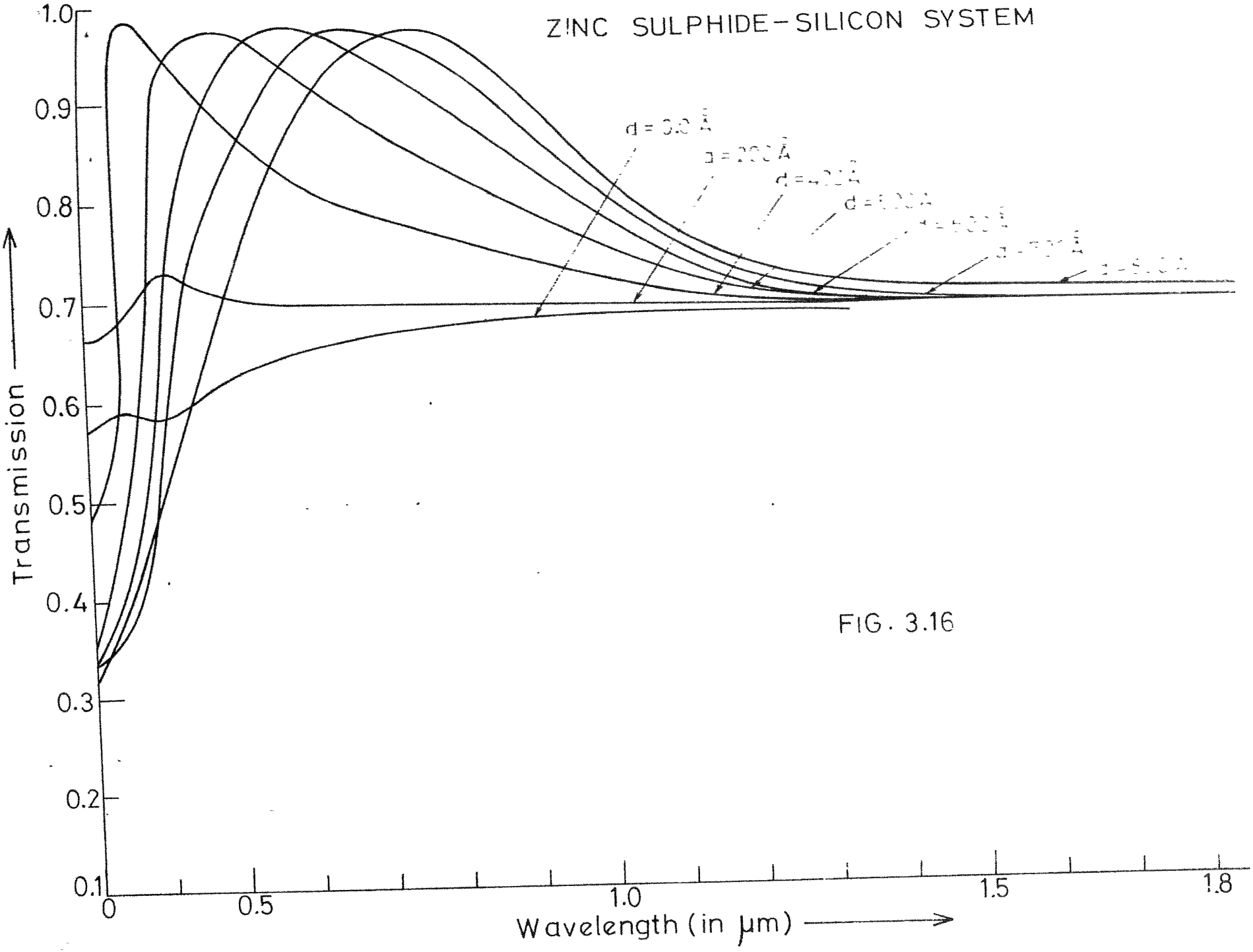
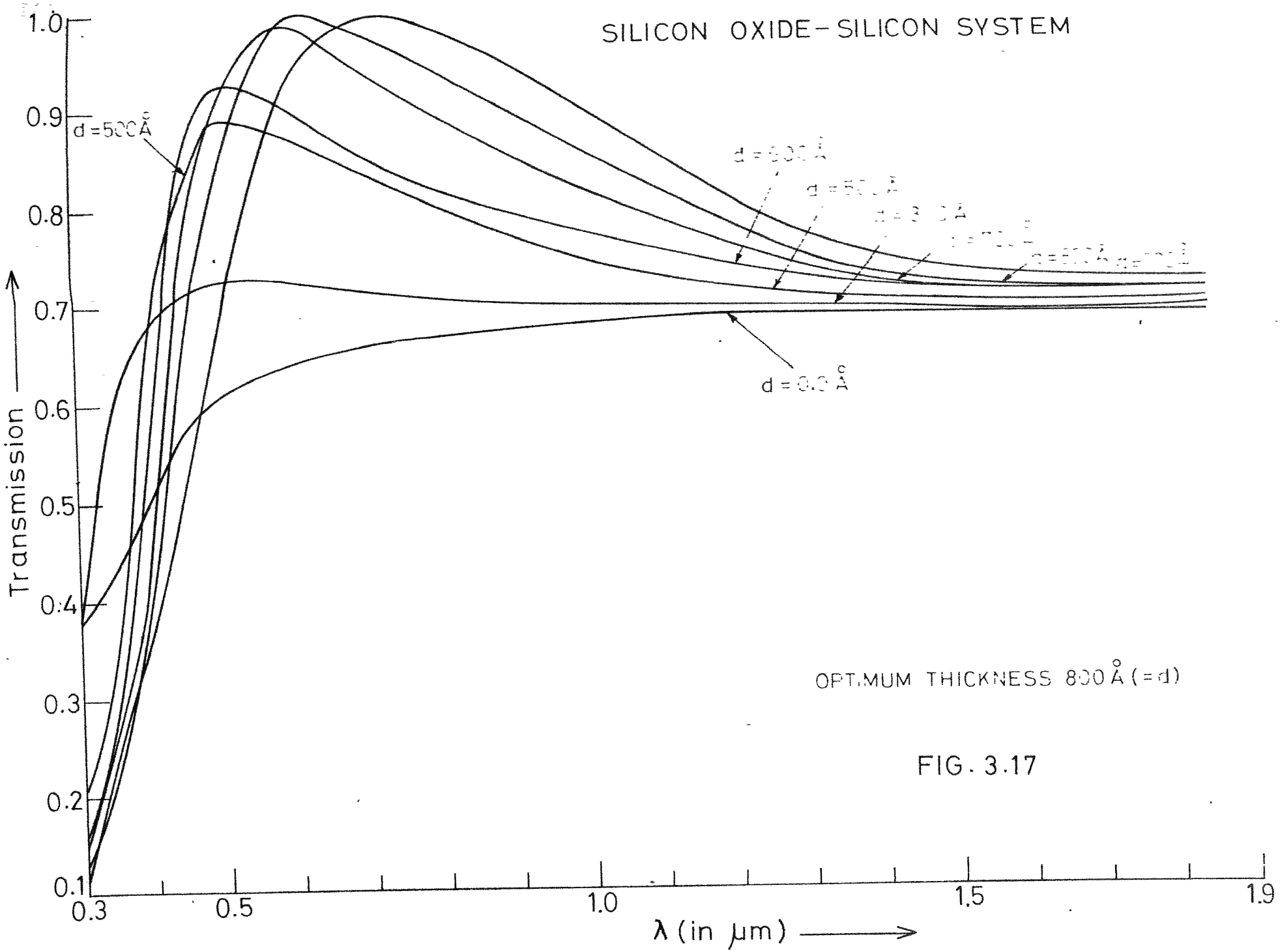

ZINC SULPHIDE-SILICON SYSTEM
Transmission
Wavelength (in μm)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.5
1.0
1.5
1.8

FIG. 3.16



OPTIMUM THICKNESS 800 Å (= d)

FIG. 3.17

It can be seen that in the total transmission, peaks are observed in a certain range of wavelengths. These peaks become broader and shift towards higher wavelength side, as the thickness (d) is increased. The maximum transmission, however, remains almost the same ($\sim 96\%$) for d in the range 500 Å to 800 Å. Also, the short wavelength response decreases and long wavelength response increases as the film thickness (d) increases. To know the optimum value of d, a knowledge of the wavelength regionx in which the high values of Tr would be most effective, is required. A look at the utilisable solar spectrum, for Si, [29] shows that this range is around .5 μm-.9 μm. Therefore, the optimum thickness d should be such that the transmittance be maximum in the wavelength region .5 μm - .9 μm. Considering the response curves for various thicknesses of the ARC, the optimum thickness turns out to be 700 Å in this case.

(ii) SiO-Si System:

A plot of transmittance versus wavelength with the thickness (d) of SiO film is given in Fig. 3.17. The nature of these curves is different from that of previous set of curves. This is because SiO is slightly absorbing in the optical region whereas ZnS was totally non-absorbing the region of interest. Here also, the peak shifts towards the long wavelength side with increase in thickness of the ARC.

But the maximum in transmission at each value of d goes down as d increases. The short-wavelength response decreases and long-wavelength response increases with increase in d.

From these curves and the considerations of the solar radiation, described earlier, the optimum value of d is found to be 800 Å.

Table 3: Optical Constants of Silicon [30].

(in μm)	n	k	(in μm)	n	k
0.30	4.65	4.08	0.70	3.82	0.008
0.35	5.25	3.00	0.75	3.75	0.005
0.40	5.5	0.26	0.80	3.72	0.003
0.45	4.65	0.10	0.85	3.70	0.002
0.50	4.30	0.05	0.90	3.65	0.001
0.55	4.05	0.02	0.95	3.64	0.000
0.60	3.94	0.015	1.00	3.60	0.000
0.65	3.88	0.01	1.50	3.50	0.000
			2.00	3.45	0.000

Table 4: Optical Constants of SiO [32].

(in μm)	n	k	(in μm)	n	k
0.30	2.20	0.45	0.70	1.96	0.00
0.35	2.27	0.25	0.75	1.95	0.00
0.40	2.15	0.15	0.80	1.94	0.00
0.45	2.05	0.10	0.85	1.935	0.00
0.50	2.00	0.04	0.90	1.93	0.00
0.55	1.985	0.02	0.95	1.915	0.00
0.60	1.97	0.00	1.00	1.90	0.00
0.65	1.965	0.00	1.50	1.89	0.00
			2.00	1.88	0.00

Table 5: Optical Constants of ZnS [31]

(in μm)	n	k	(in μm)	n	k
0.30	2.81	0.28	0.70	2.32	0.00
0.35	2.60	0.185	0.75	2.32	0.00
0.40	2.50	0.00	0.80	2.32	0.00
0.45	2.43	0.00	0.85	2.32	0.00
0.50	2.384	0.00	0.90	2.32	0.00
0.55	2.36	0.00	0.95	2.32	0.00
0.60	2.332	0.00	1.00	2.32	0.00
0.65	2.324	0.00	1.50	2.32	0.00
			2.00	2.32	0.00

CHAPTER IV

DISCUSSION ON THE EFFICIENCY OF THE SYSTEM

In this section, the theoretical results for the optimum cell performance are discussed under the constraints of technical difficulties.

The calculations, done in sec. 3.5, show that for L/B ratio greater than 54, the efficiency of the lateral SBSC can be enhanced above that of the conventional SBSC. However, with the limitation on the maximum allowable value of grid spacing (L) ($L \leq 2L_n$; L_n: minority carrier diffusion length), the corresponding value of grid width (B), for such large L/B ratios, becomes very small. Obtaining submicron values of B is technically very difficult. In photolithography, due to long wavelength radiation (300-450 nm) employed and due to other process limitations, 2.4 μm metal widths are the smallest that can readily be delineated. Electron-lithography has been tried to produce features less than .01 μ [33]. Therefore, grid spacing (L) must be determined as a compromise between the required cell performance and the cost of fabrication.

The thickness of the grid strips is a very crucial parameters in determining its contribution to the series

resistance of the cell. A very thick metal-film is desirable for the low resistance of the grid strips. But the process of 'undercutting', as explained in sec. 2.3, puts a restriction on the maximum thickness of the film. In fact, undercutting allows no grid widths smaller than about twice the film thickness using chemical etching. Recently, Sputter etching techniques have been used [34] for grid widths of the order of the thickness of the film. Therefore, the thickness of the grid strips should be such that the 'undercutting' does not pose any problem.

The parasitic role of surface recombination limits the present structure to silicon only. In the next best studied material, GaAs, the value of surface recombination velocity, which is a direct measure of surface recombination, is very high (10^6 cms/sec) whereas for silicon it is only 10^3 cms/sec. This bars the use of GaAs for such a structure. Furthermore, special precautions have to be taken to reduce the surface recombination as much as possible. This may done by introducing proper electric fields near the surface of the semiconductors through suitable doping variations.

The process of heat treatment not only improves the adhesion of the film to a large extent but also increases the barrier height of the Al-Si system (n-type Si). This has been shown by Basterfield etal.[35]. The barrier may be

raised from .68 eV to .74 eV by giving a heat treatment to the Al-Si system at 500°C and then cooling it at a rate of 2°C/min. The ideality factor (n) also increases at the same time. This has been attributed to the dissolution of silicon in aluminium, during the heat treatment, which on cooling recrystallises on to the lightly doped n-type silicon as an aluminium doped p-type layer. An increase in the barrier height and the ideality factor, as shown earlier, would provide an increased open circuit voltage and hence better overall efficiency of the cell. Of course, the extra process of heat treatment adds to the cost of fabrication. Furthermore, special care has to be taken to avoid any possible oxidation of aluminium to aluminium oxide. This would form an insulating layer on the aluminium film and, thus, prevent it from making any contact with the external lead.

The extra process of photolithography can altogether, be avoided by evaporating the metal through a mask. However, such fine geometries can not be made through ordinary tools and, therefore, special methods are to employed.

The present fabrication process is not quite suitable for p-type silicon. This is because, as described in sec.2.4, it does not allow any heat treatment for better adhesion. An evaporation through a metal mask could be a better choice for p-type silicon.

APPENDIX I

SOLUTION OF CONTINUITY EQUATION IN ILLUMINATED REGION

The continuity equation for the illuminated region (cf. Fig. 1) is expressed as,

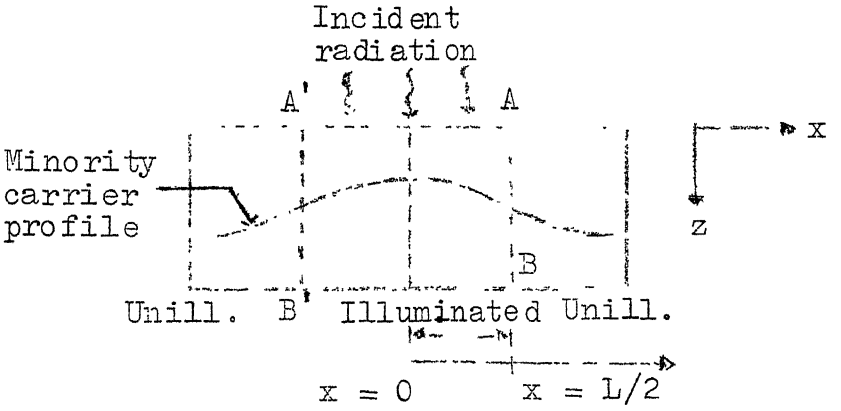


Fig. 1.

$$D_n \frac{d^2 n1}{dx^2} - \frac{n1}{\tau_n} + N \alpha_x e^{-\alpha z} = 0 \qquad (1)$$

It has a solution of the form,

$$n1 = C_1 e^{x/L_n} + C_2 e^{-x/L_n} + N \alpha e^{-\alpha z} \cdot \tau_n \; ; \quad 0 \leq x \leq L/2 \qquad (2)$$

The electron current in this region is given by,

$$J_n = qD_n \cdot \frac{d_{n1}}{dx}$$

$$= \frac{q D_n}{L_n} [C_1 e^{x/L_n} - C_2 e^{-x/L_n}] \quad 0 < x < L/2 \qquad (3)$$

Now, the symmetry around x = 0 demands that the electron current must vanish at x = 0.

Therefore, we find that the condition,

$$J_n = 0 \quad \text{at } x = 0$$

requires,

$$C_1 = C_2 \tag{4}$$

and the solution (3) becomes,

$$J_n = \frac{2qD_n C_1}{L_n} \cdot \text{Sin h } \frac{x}{L_n} ; \quad 0 < x < L/2 \tag{5}$$

The continuity equation in the region not exposed to light (cf. Fig. 1), would be given by,

$$D_n \frac{d^2 nl}{dx^2} - \frac{nl}{\tau_n} = 0 \qquad x > L/2 \tag{6}$$

Since, the solution of (6) must vanish at x = + ,

$$nl = 0 \quad \text{at} \quad x = + \infty \tag{7}$$

This gives,

$$nl = B e^{-x/L_n} ; \quad x > L/2 \tag{8}$$

The corresponding electron current density would be given by,

$$J_n = - \frac{qD_n}{L_n} B e^{-x/L_n} ; \quad x > L/2 \tag{9}$$

Now, at plane $x = L/2$, the hole currents given by eqn. (5) and (9) must agree. Therefore,

$$-B\, e^{-L/2L_n} = \frac{2C_1}{L_n} \operatorname{Sin\,h} \frac{L}{2L_n}$$

or,

$$B = C_1 \left(1 - e^{L/2\, L_n}\right) \tag{10}$$

But, at the plane $x = L/2$, the electron concentration should also agree. Because a discontinuity in electron concentration would mean infinite current at $x = L/2$. Therefore, from eqns. (8), (10), (2), and (4), we find that at $x = L/2$.

$$C_1\left(1 - e^{L/2L_n}\right) e^{-L/2L_n} = C_1\left(e^{L/2L_n} + e^{-L/2L_n}\right) + N\alpha e^{-\alpha z} \cdot \tau_n$$

or,

$$C_1 = -\frac{N\alpha e^{-\alpha z/L_n}}{2} \cdot e^{-L/2L_n}$$

Therefore, the solution of eqn. (1) may be written as follows,

$$n1 = N\alpha e^{-\alpha z} \cdot \tau_n \left[1 - e^{-L/2L_n} \operatorname{Cos\,h} \frac{x}{L_n}\right]$$

$$J_{n1} = q\, N\alpha e^{-\alpha z}\, L_n\, e^{-L/2L_n} \cdot \operatorname{Sin\,h} \frac{x}{L_n} \qquad 0 \leq x \leq L/2$$

APPENDIX II

SOLUTION OF CONTINUITY EQUATION IN UNILLUMINATED REGION

As has been described in Sec. 3.3, the continuity equation in the unilluminated region would be given by,

$$D_n \frac{d^2 n2}{dz^2} - \frac{n2}{\tau_n} + \chi \frac{e^{-\alpha z}}{B/2} = 0 \qquad (1)$$

where $\chi = N(\lambda)\, \alpha(\lambda)\, L_n \,\text{Sin h}\, L/2L_n .\, e^{-L/2L_n}$

It has the solution of the term,

$$n2 = C_1 e^{z/L_n} + C_2 e^{-z/L_n} + \frac{\chi\, e^{-\alpha z}}{D_n \left[\frac{1}{L^2} - \alpha^2 \right) \frac{B}{2}} \qquad (2)$$

where C_1 and C_2 are the constants to be determined from the boundary conditions given below:

at $z = 0$, $n2 = 0$

at $z = \infty$, $D_n \frac{d n2}{dz} = 0$

From the second boundary condition and eqn. (2) we get,

$$C_1 = 0 \qquad (3)$$

From the first boundary condition and eqn. (2) we get,

$$C_2 + \frac{\chi}{\frac{B}{2} D_n \left(\frac{1}{L_n^2} - \alpha^2 \right)} = 0 \qquad (4)$$

Therefore, the solution may be written as,

$$n2 = \frac{\chi}{D_n \left(\frac{1}{L_n^2} - \alpha^2\right) \frac{B}{2}} \left(e^{-\alpha z} - e^{-z/L_n}\right) \qquad (5)$$

and,

$$J_{n2} = q D_n \frac{D_{n1}}{dz} = \frac{q \cdot \chi}{\left(\frac{1}{L_n^2} - \alpha^2\right) \frac{B}{2}} \left(\frac{1}{L_n} e^{z/L_n} - \alpha e^{-\alpha z}\right) \qquad (6)$$

at the MS junction i.e. $z = 0$ we have,

$$J_{n2} = q D_n \frac{d_{n2}}{dz}\Big|_{z=0} = \frac{q \cdot \chi}{\left(\frac{1}{L_n} + \alpha\right) \frac{B}{2}} \qquad (7)$$

Now, if we integrate $q\, g_L(z)\, e^{-z/L_n}$ over z (as described in sec. 3.3), we have,

$$q\chi \int_0^\infty g_L(z)\, e^{-z/L_n}\, dz = \frac{q\chi}{B/2} \int_0^\infty e^{-(\alpha + 1/L_n)z}\, dz$$

$$= \frac{q\chi}{(\alpha + 1/L_n) \frac{B}{2}} \qquad (8)$$

Thus, we see that eqn. (7) and eqn. (8) are exactly same.

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